FIG. 1

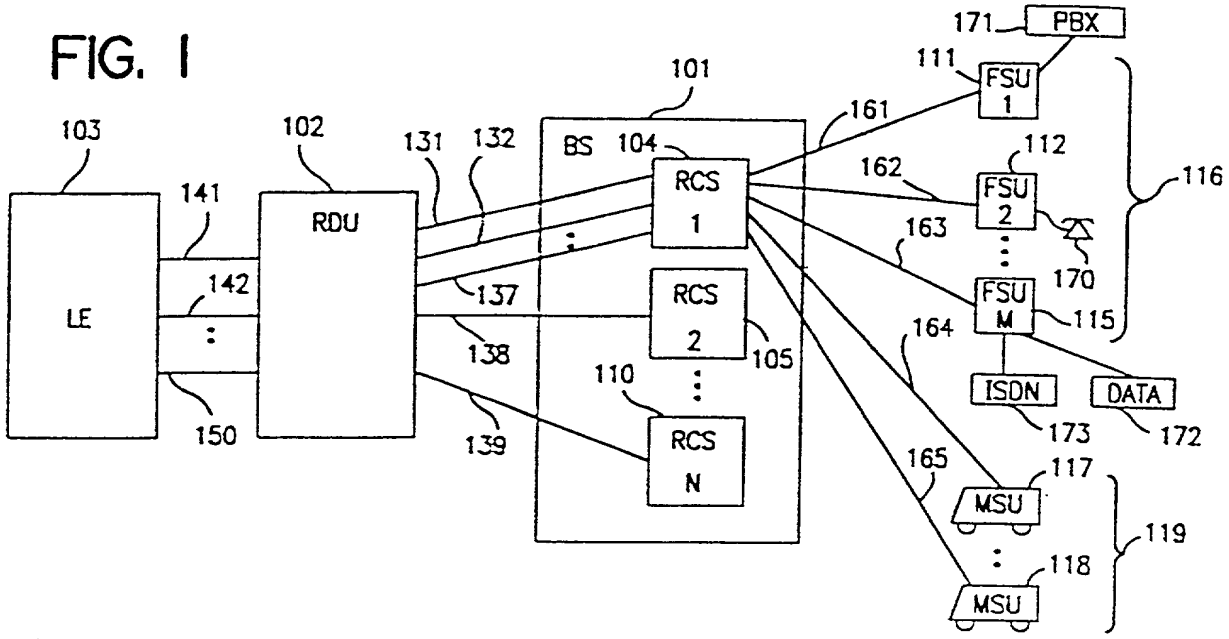


FIG. 2a

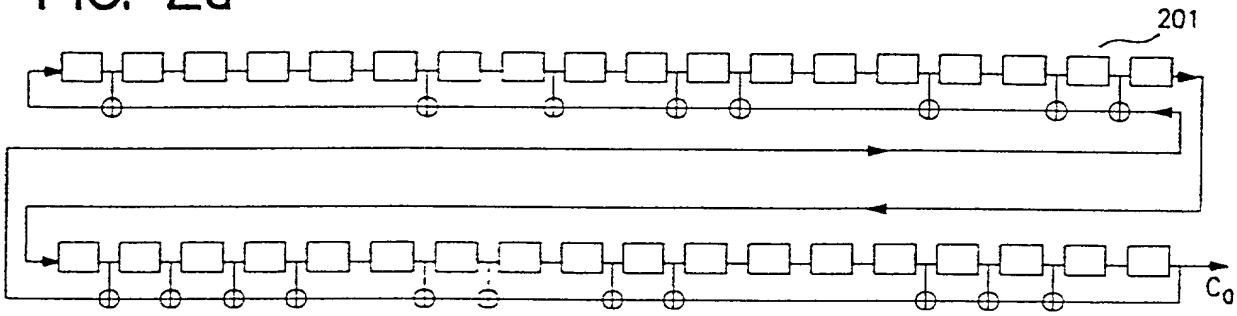


FIG. 2b

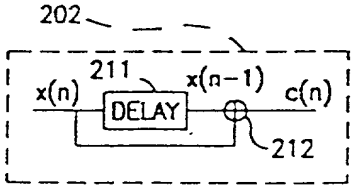
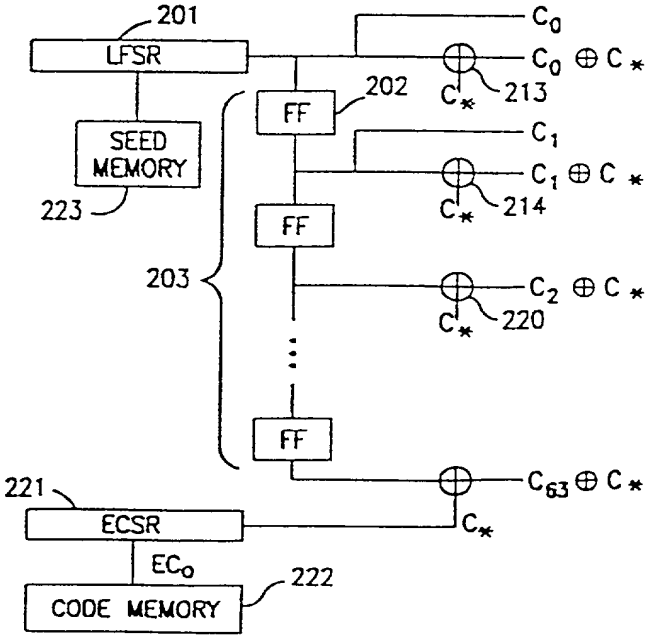


FIG. 2c



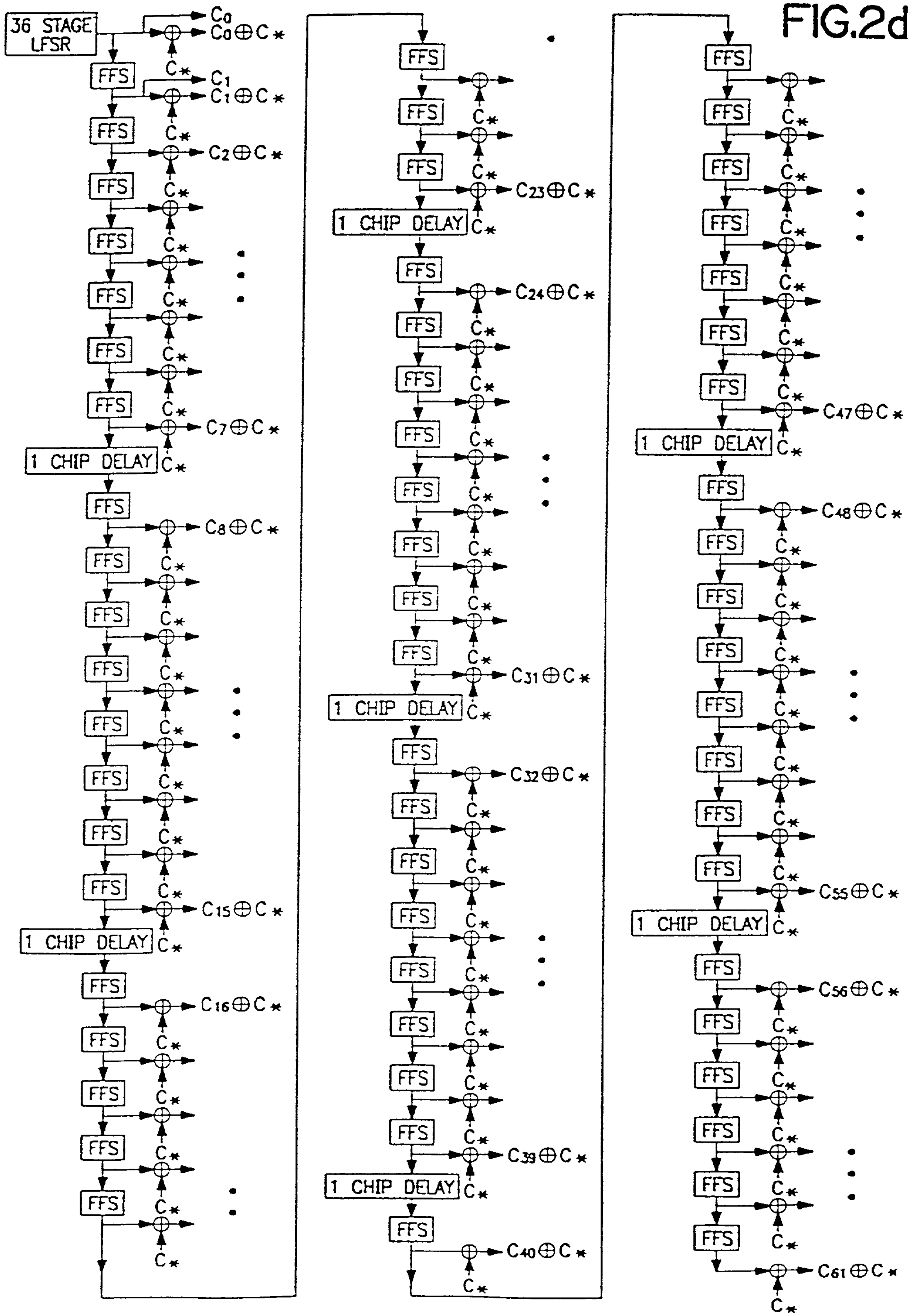

36 STAGE LFSR
FFS
1 CHIP DELAY
C0
C0⊕C*
C1
C1⊕C*
C2⊕C*
C7⊕C*
C8⊕C*
C15⊕C*
C16⊕C*
C23⊕C*
C24⊕C*
C31⊕C*
C32⊕C*
C39⊕C*
C40⊕C*
C47⊕C*
C48⊕C*
C55⊕C*
C56⊕C*
C61⊕C*
C*

FIG.2d

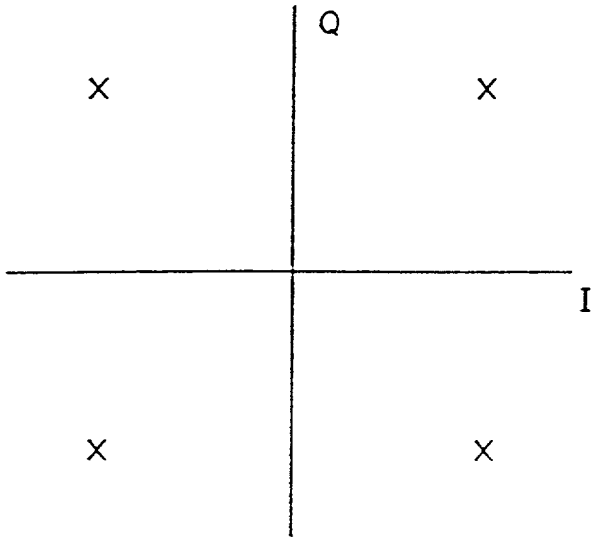


FIG. 3a

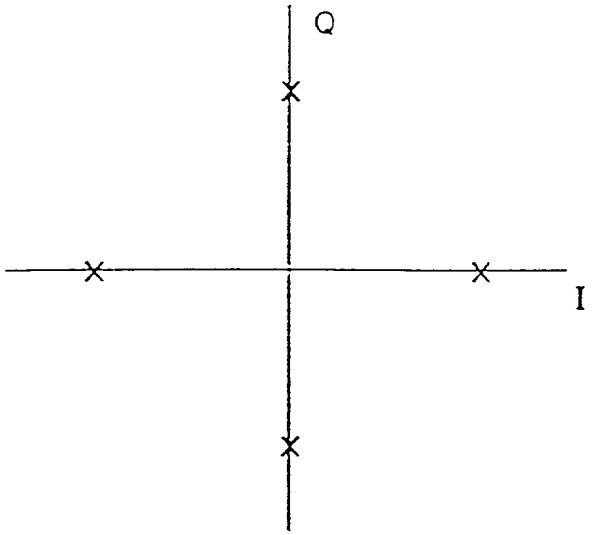


FIG. 3b

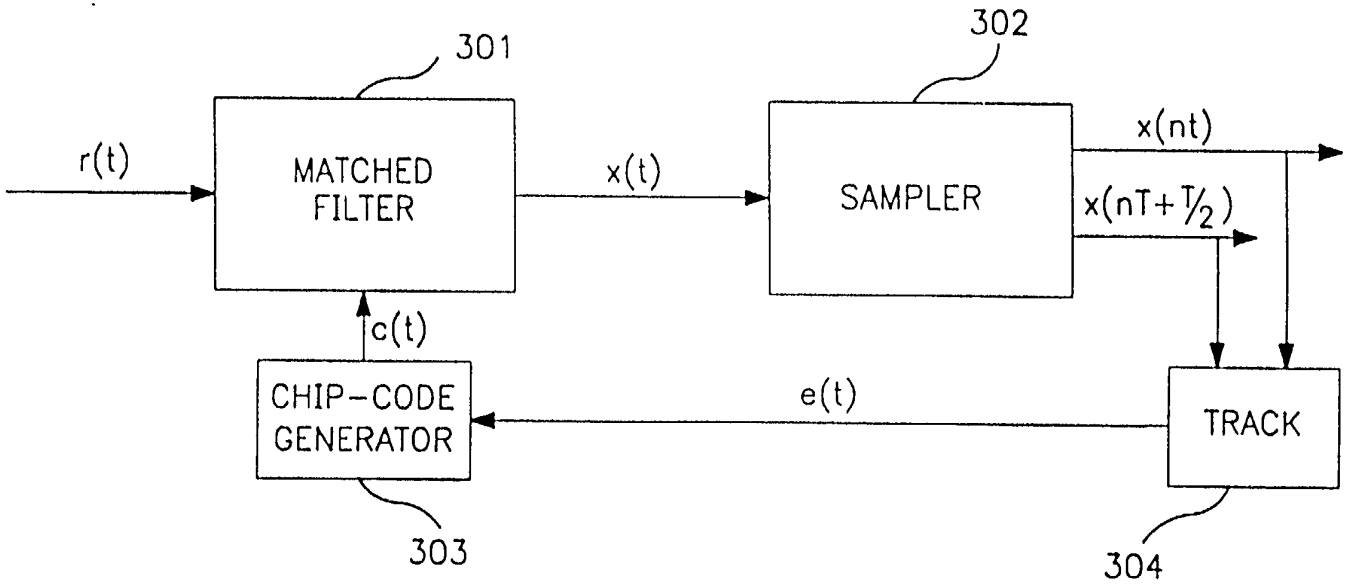


FIG. 3c

FIG. 4

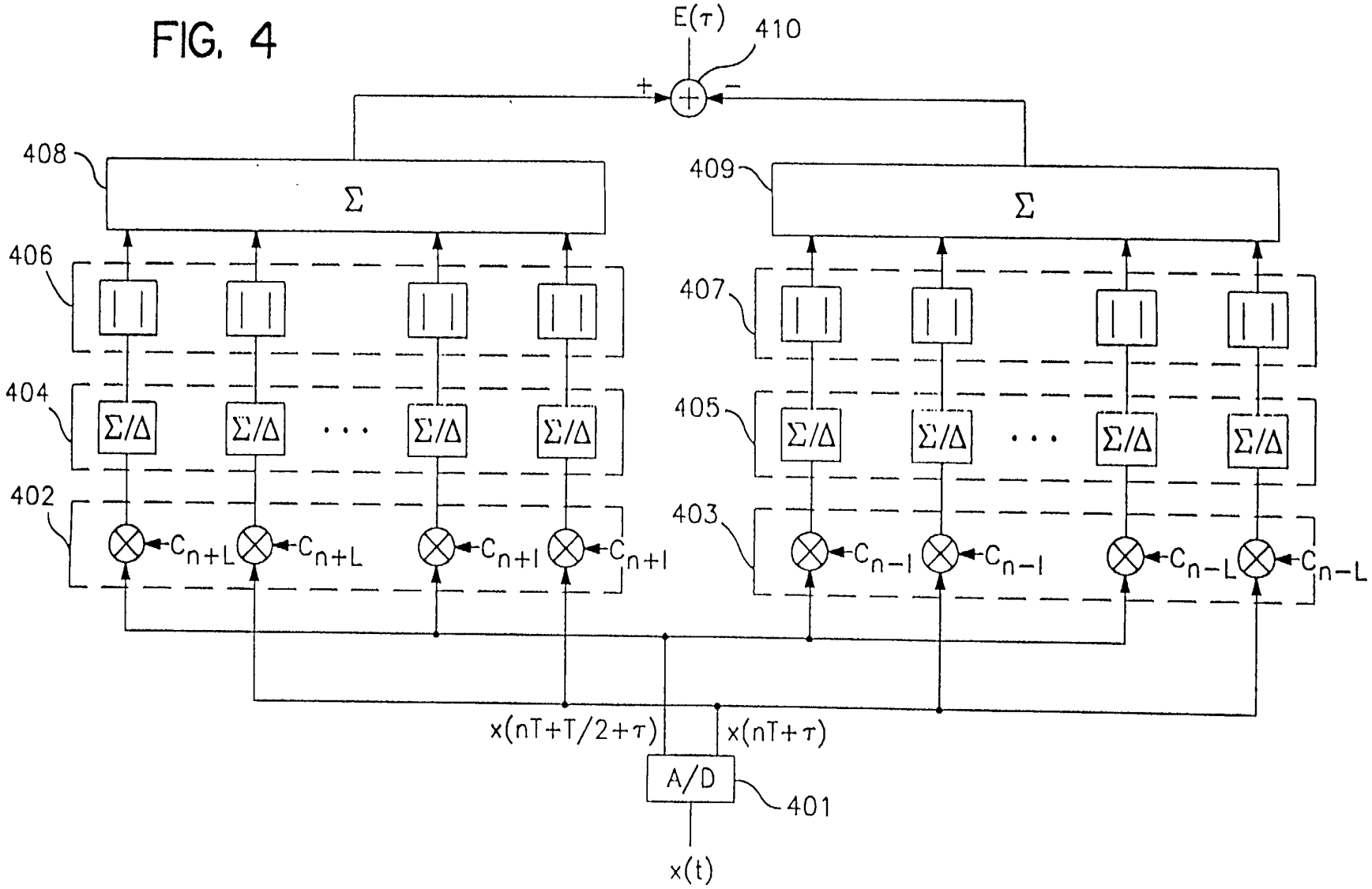


FIG. 5a

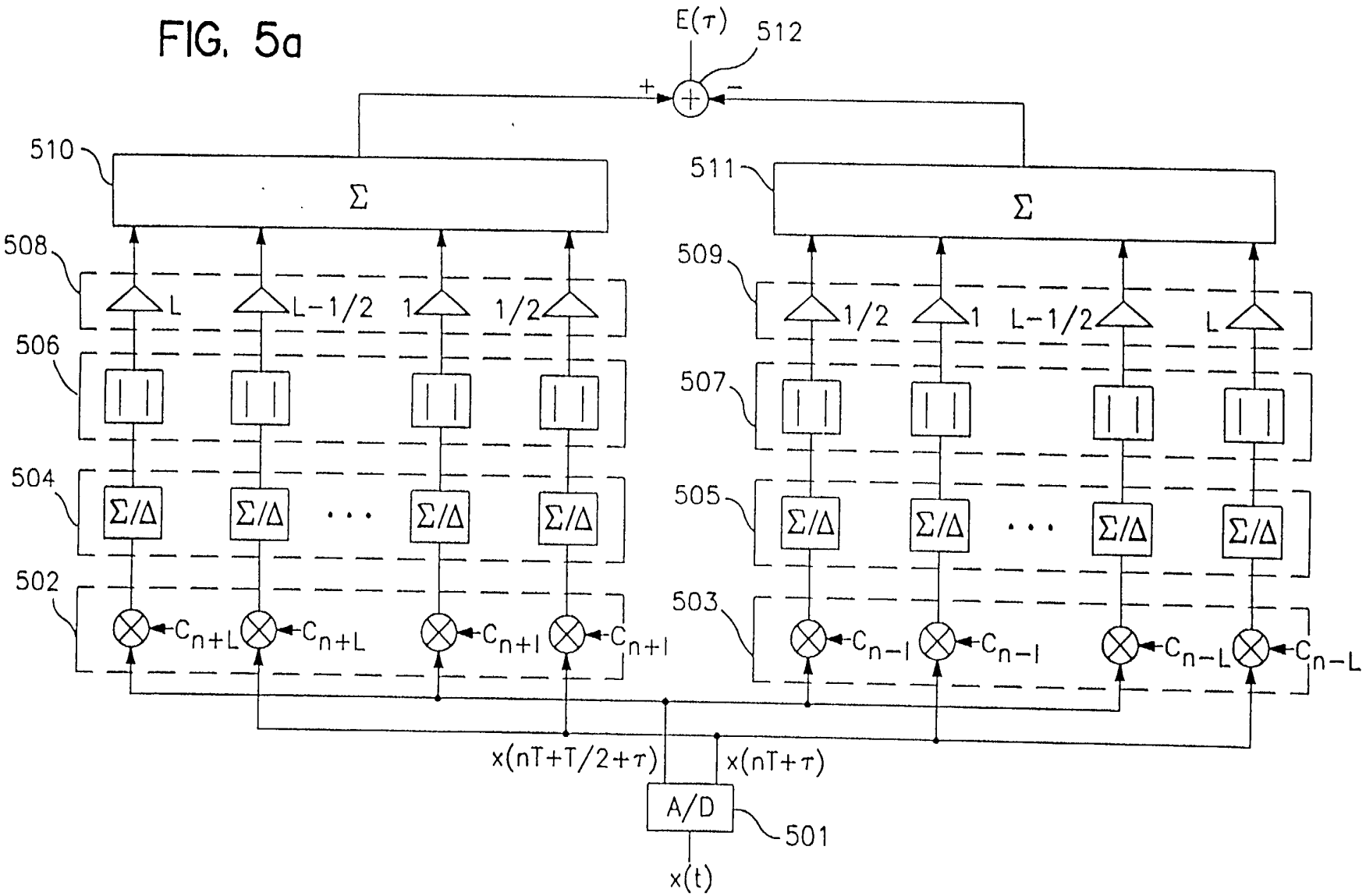
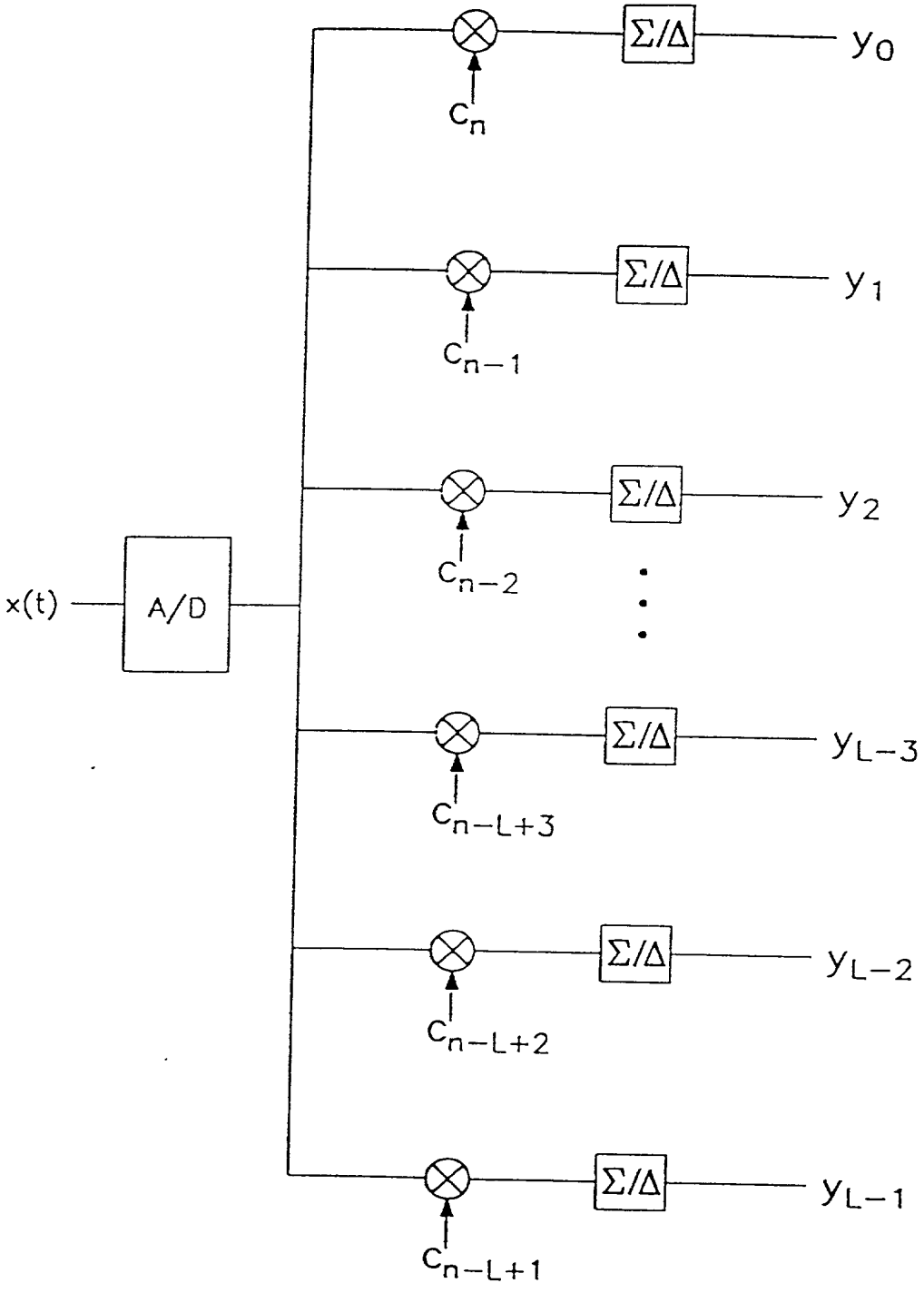

E(τ)
512
+
−
510
511
Σ
Σ
508
509
L
L−1/2
1
1/2
1/2
1
L−1/2
L
506
507
504
505
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
502
503
Cn+L
Cn+L
Cn+1
Cn+1
Cn−1
Cn−1
Cn−L
Cn−L
x(nT+T/2+τ)
x(nT+τ)
A/D
501
x(t)

FIG. 5b



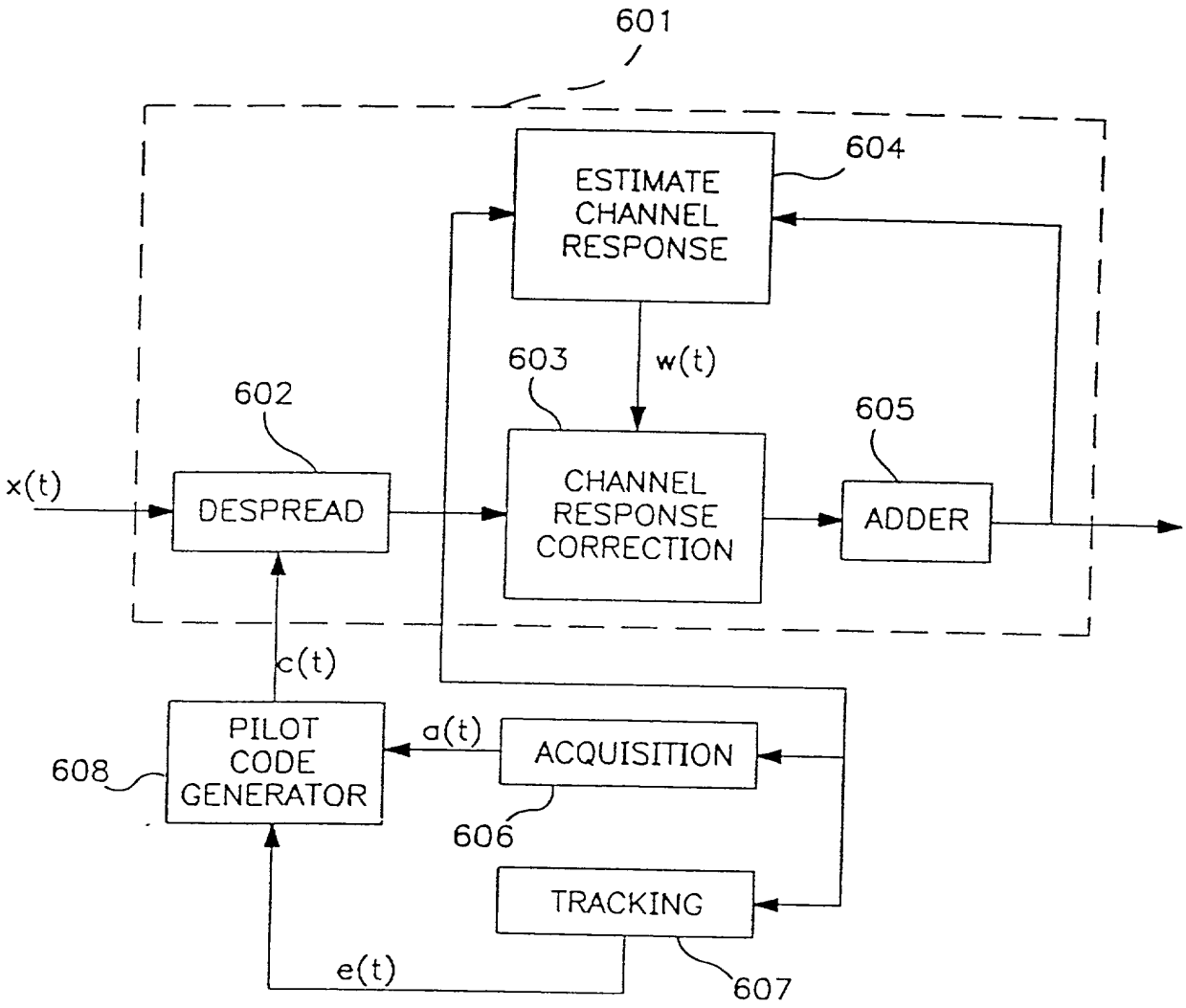

601
604
ESTIMATE CHANNEL RESPONSE
603
w(t)
602
605
x(t)
DESPREAD
CHANNEL RESPONSE CORRECTION
ADDER
c(t)
PILOT CODE GENERATOR
608
a(t)
ACQUISITION
606
TRACKING
e(t)
607

FIG. 6

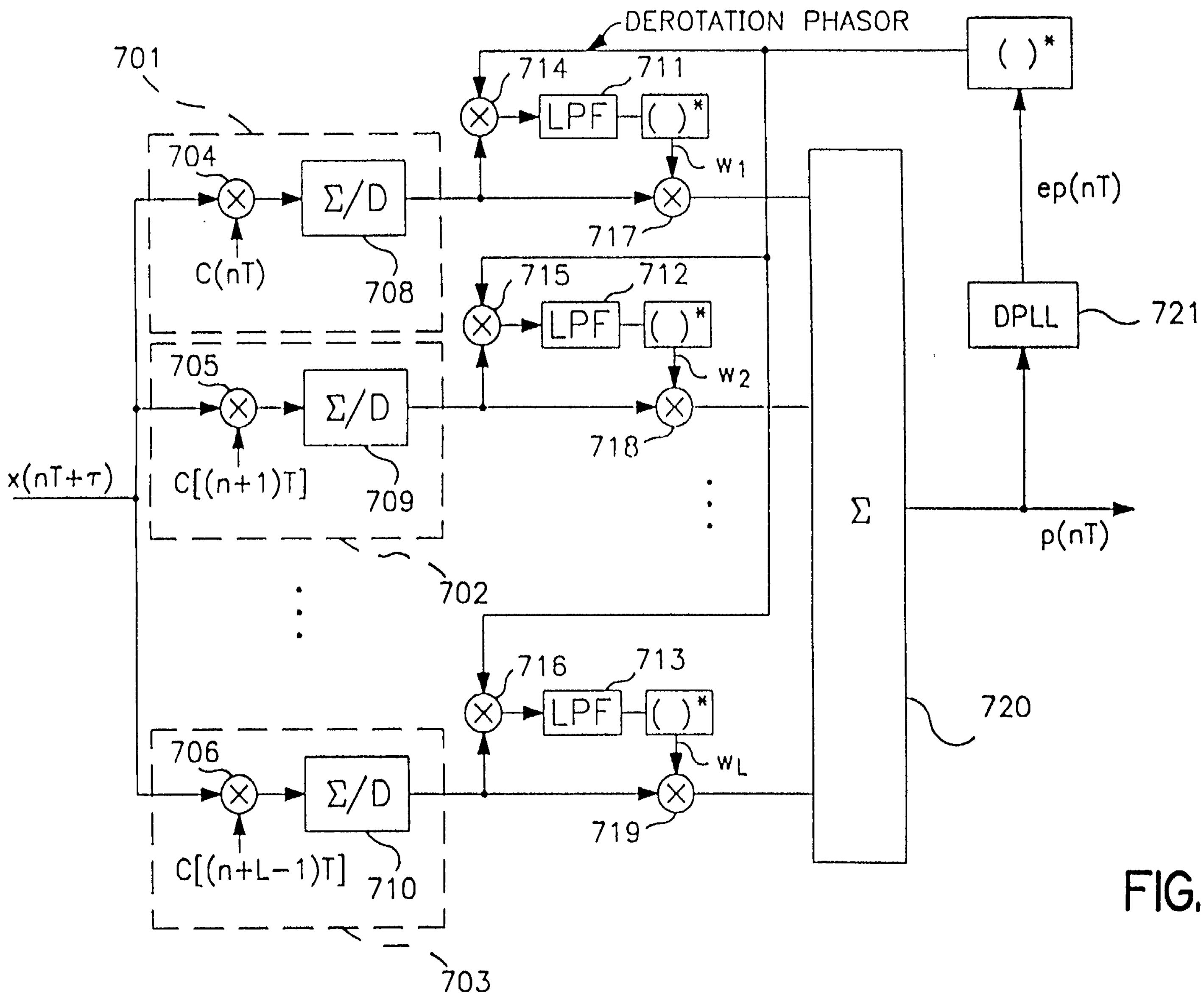

DEROTATION PHASOR
( )*
701
704
C(nT)
Σ/D
708
714
711
LPF
( )*
w1
717
705
C[(n+1)T]
Σ/D
709
715
712
LPF
( )*
w2
718
702
706
C[(n+L−1)T]
Σ/D
710
716
713
LPF
( )*
wL
719
703
x(nT+τ)
Σ
720
DPLL
721
ep(nT)
p(nT)

FIG. 7

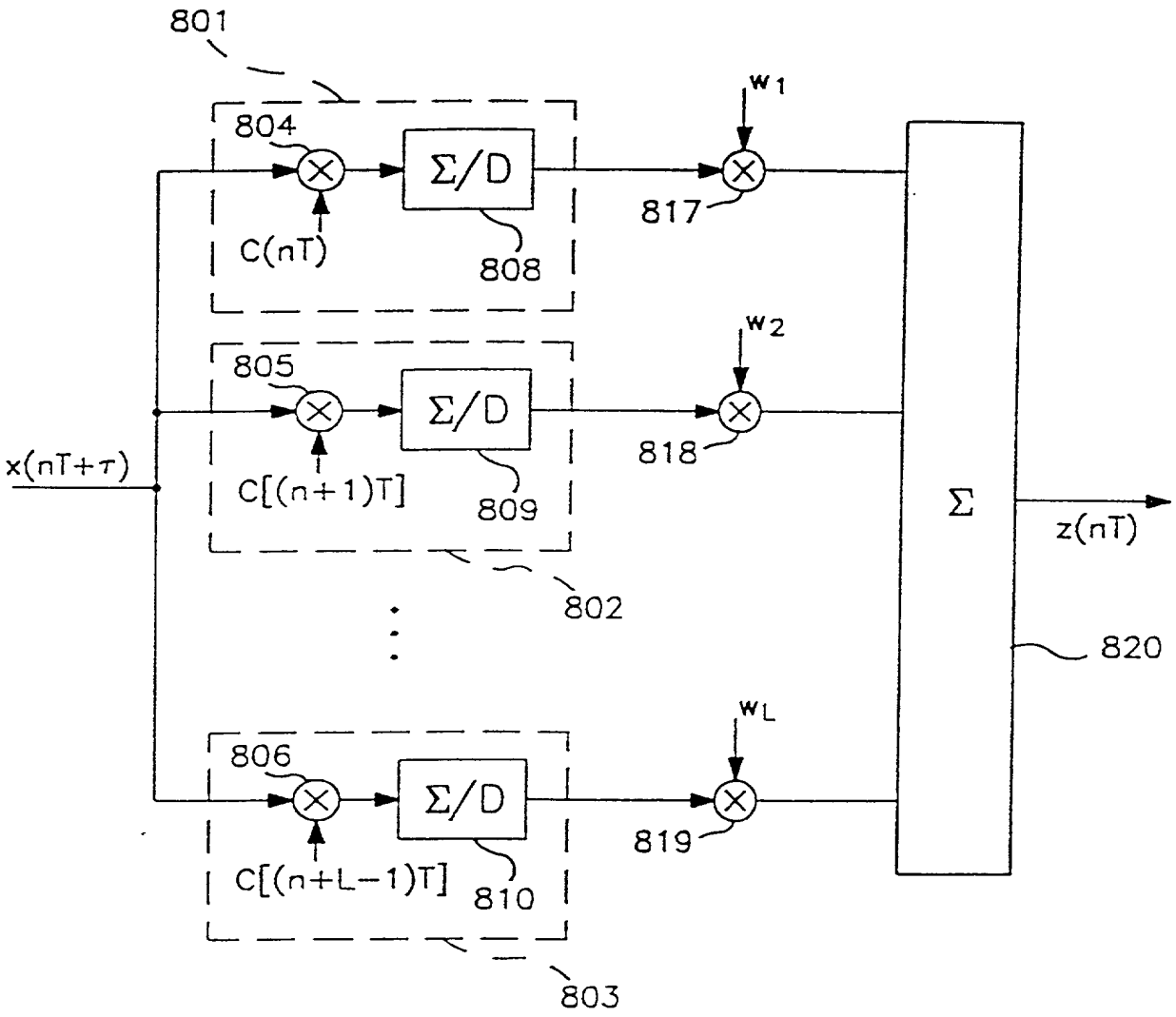

801
804
C(nT)
Σ/D
808
817
w1
805
C[(n+1)T]
Σ/D
809
818
w2
x(nT+τ)
802
806
C[(n+L−1)T]
Σ/D
810
819
wL
803
Σ
z(nT)
820

FIG. 8a

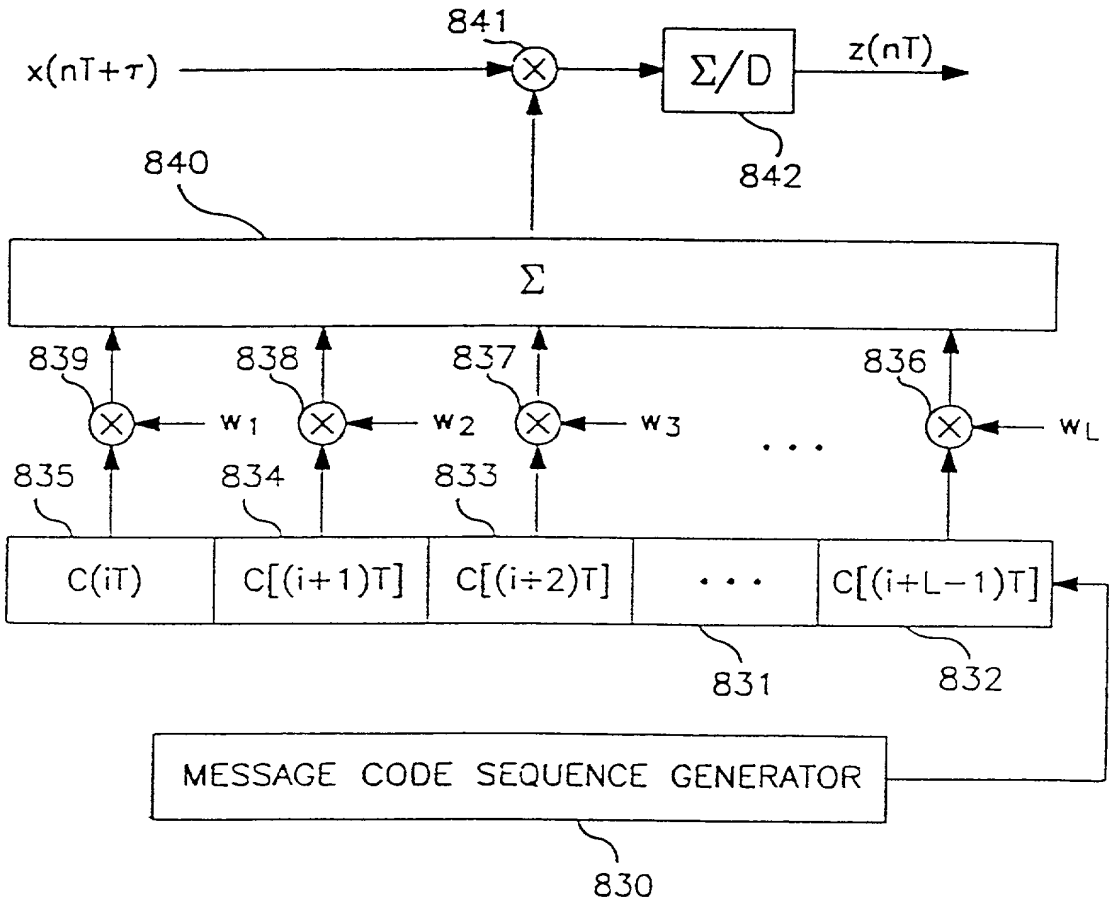


FIG. 8b

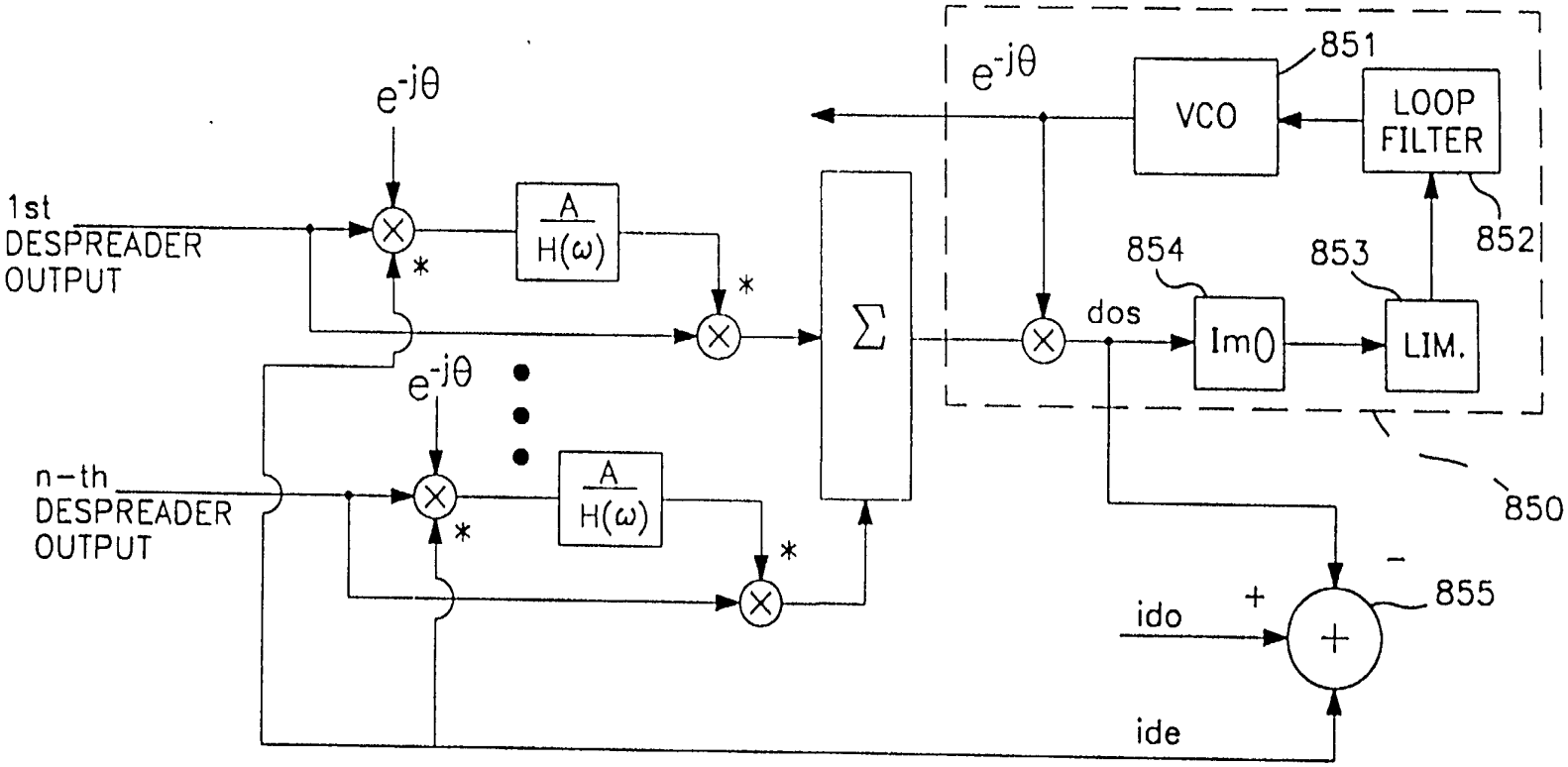

1st
DESPREADER
OUTPUT
n-th
DESPREADER
OUTPUT
e-jθ
e-jθ
e-jθ
A
H(ω)
A
H(ω)
*
*
*
*
Σ
VCO
LOOP
FILTER
851
852
853
854
dos
Im()
LIM.
850
ido
ide
+
−
855

FIG. 8c

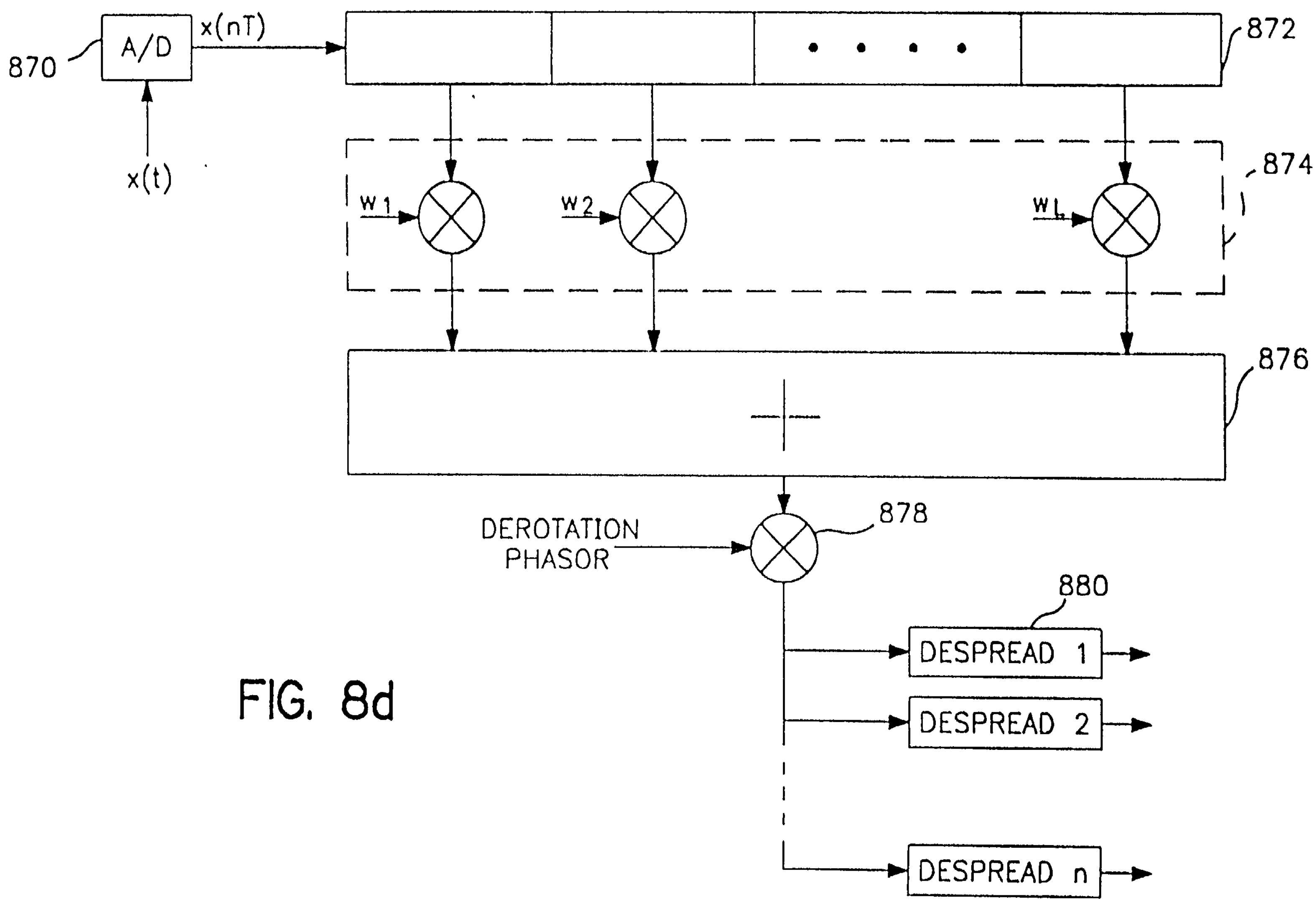


FIG. 8d

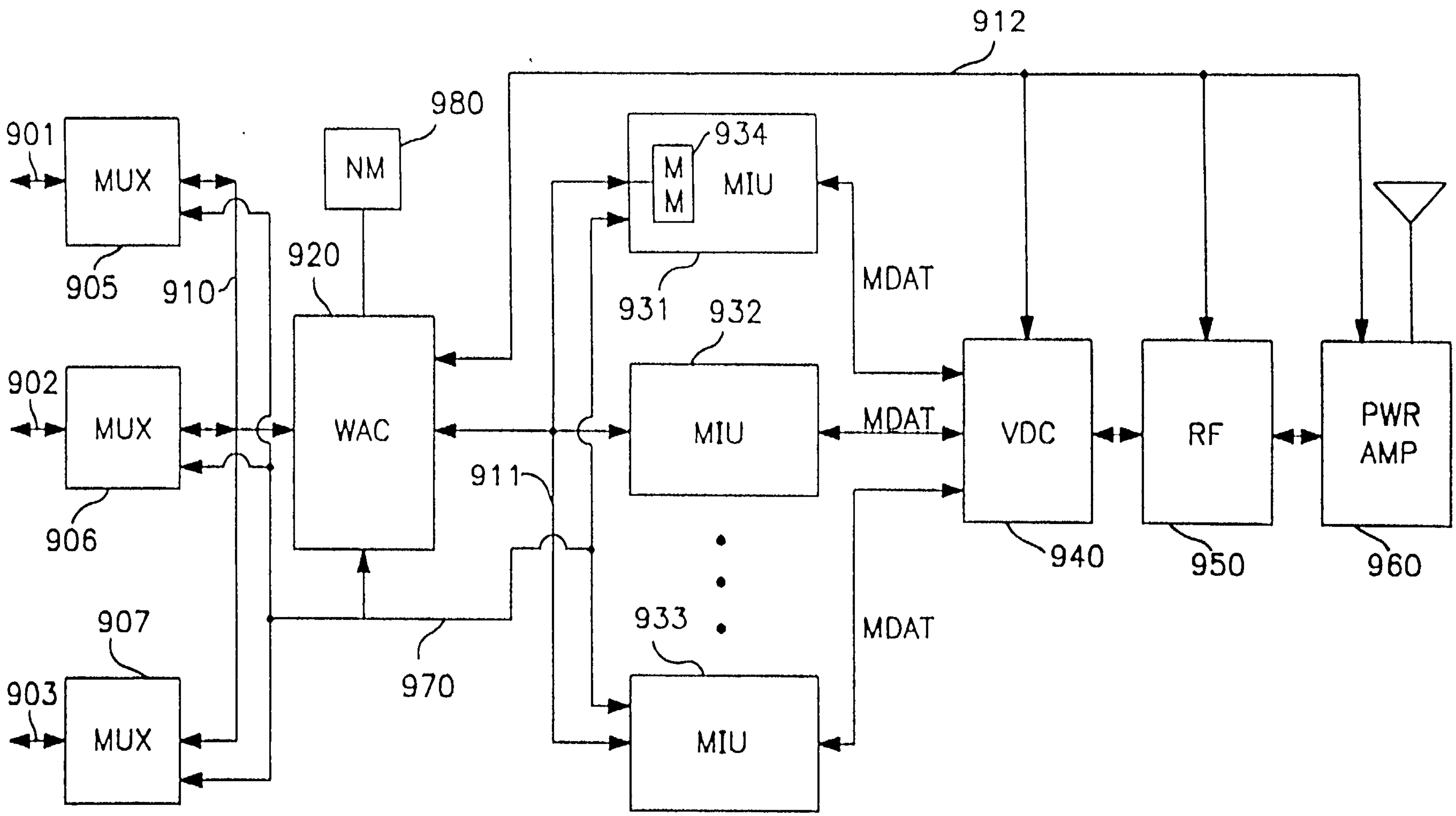

901
MUX
905
902
MUX
906
907
903
MUX
910
980
NM
920
WAC
970
911
912
934
M
M
MIU
931
932
MIU
933
MIU
MDAT
MDAT
MDAT
VDC
940
RF
950
PWR
AMP
960

FIG. 9

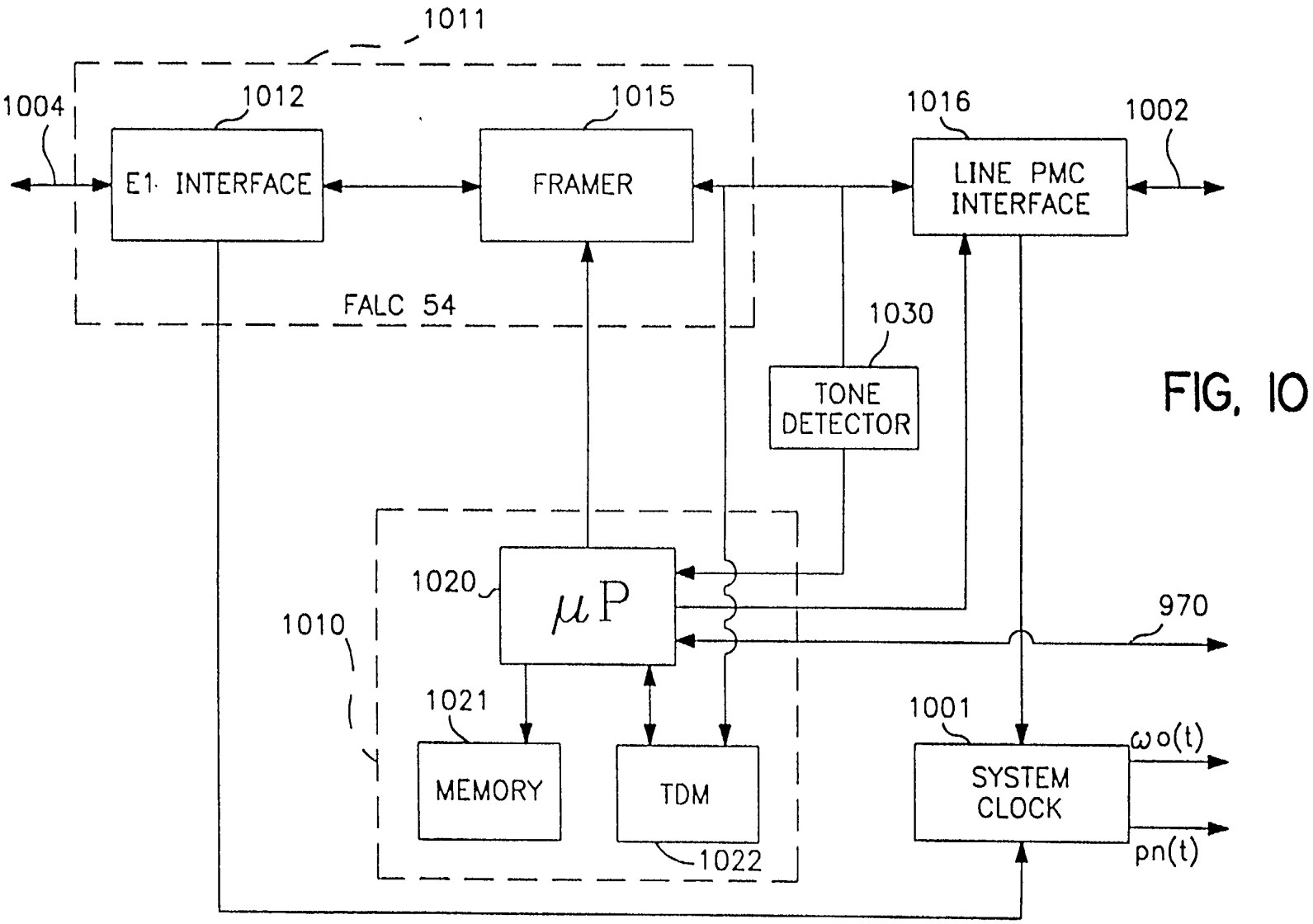

1011
1004
1012
1015
1016
1002
E1 INTERFACE
FRAMER
LINE PMC INTERFACE
FALC 54
1030
TONE DETECTOR
1020
μP
1010
970
1021
1001
MEMORY
TDM
SYSTEM CLOCK
ωo(t)
pn(t)
1022

FIG. 10

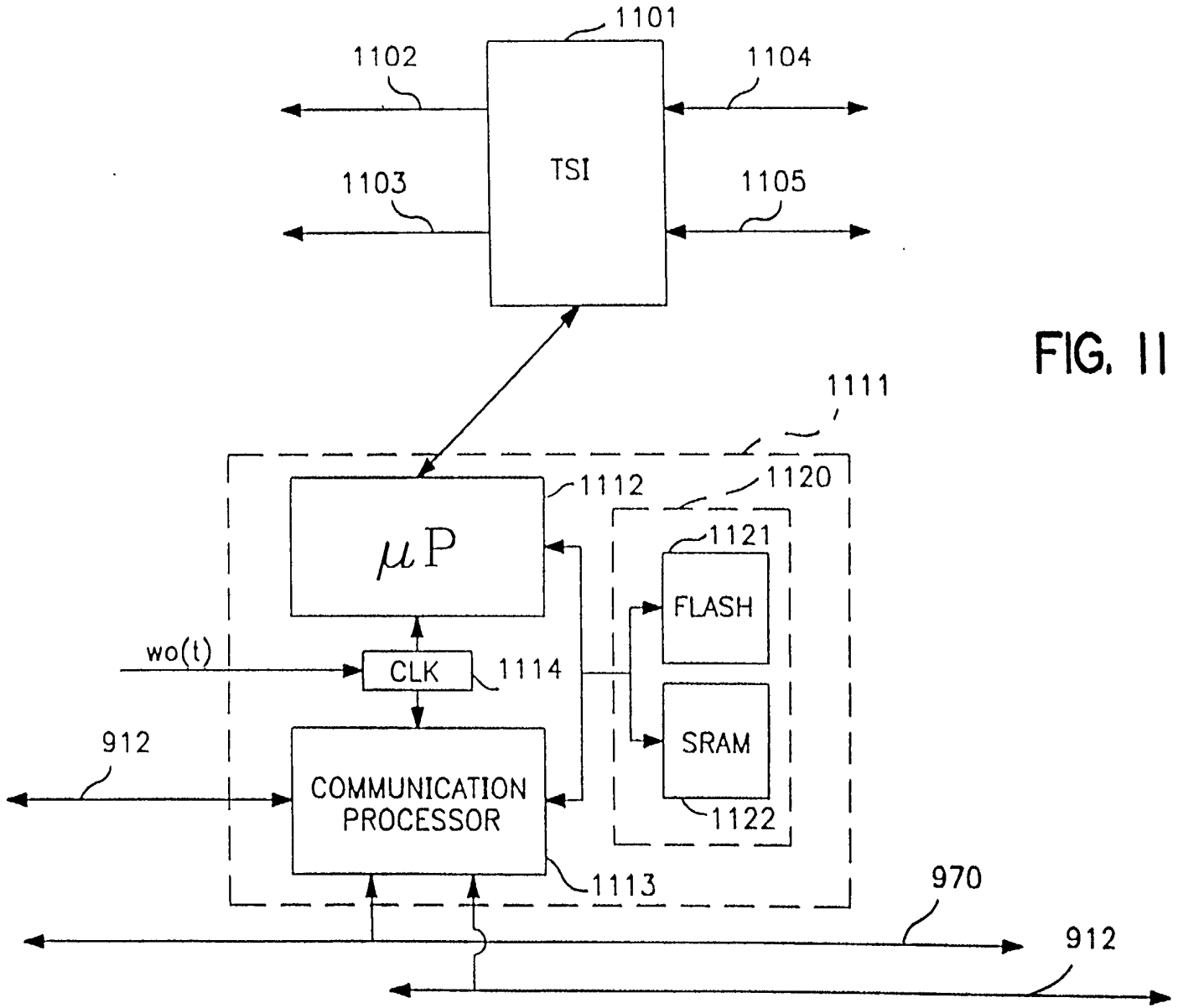


FIG. 11

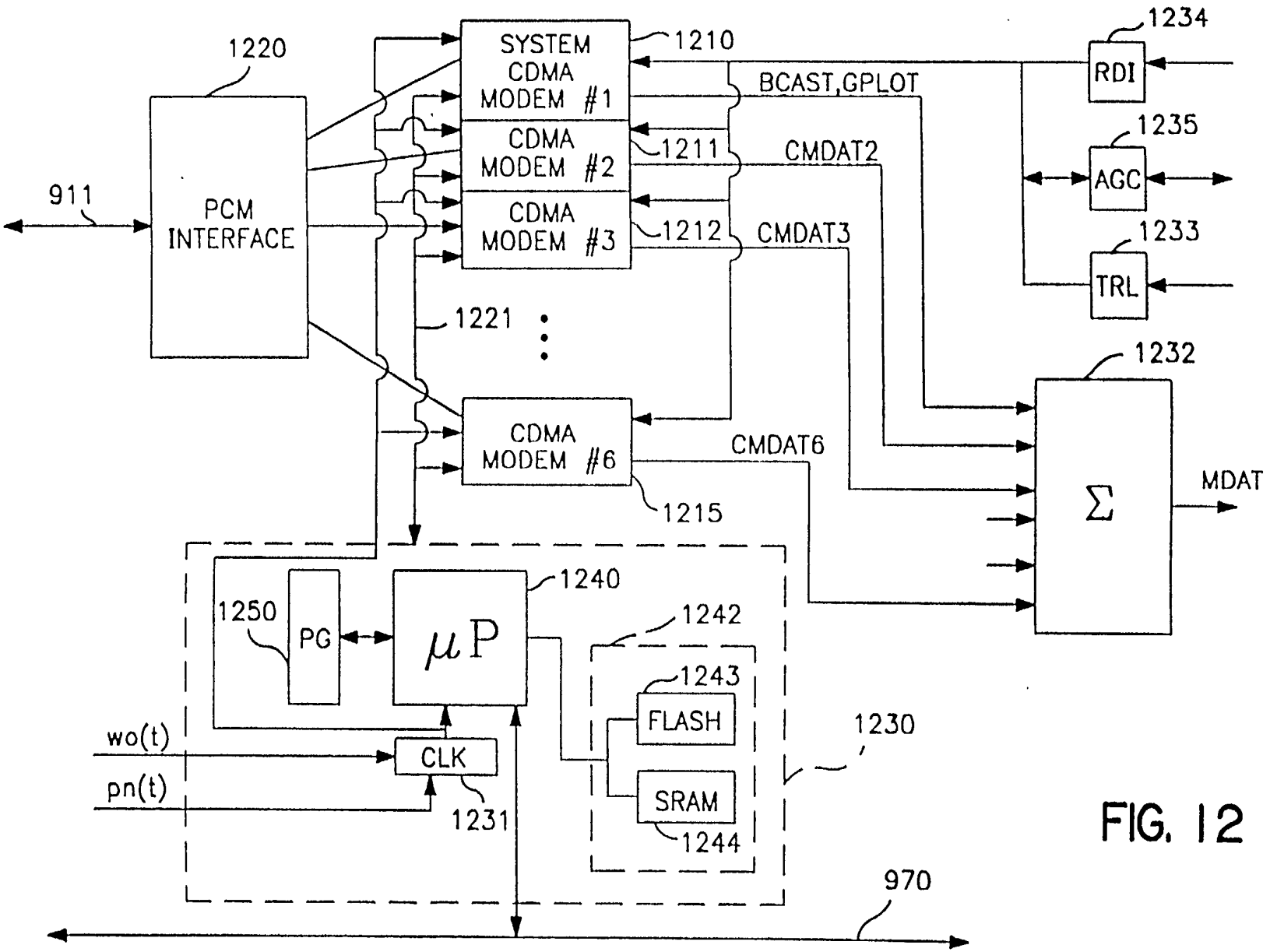


FIG. 12

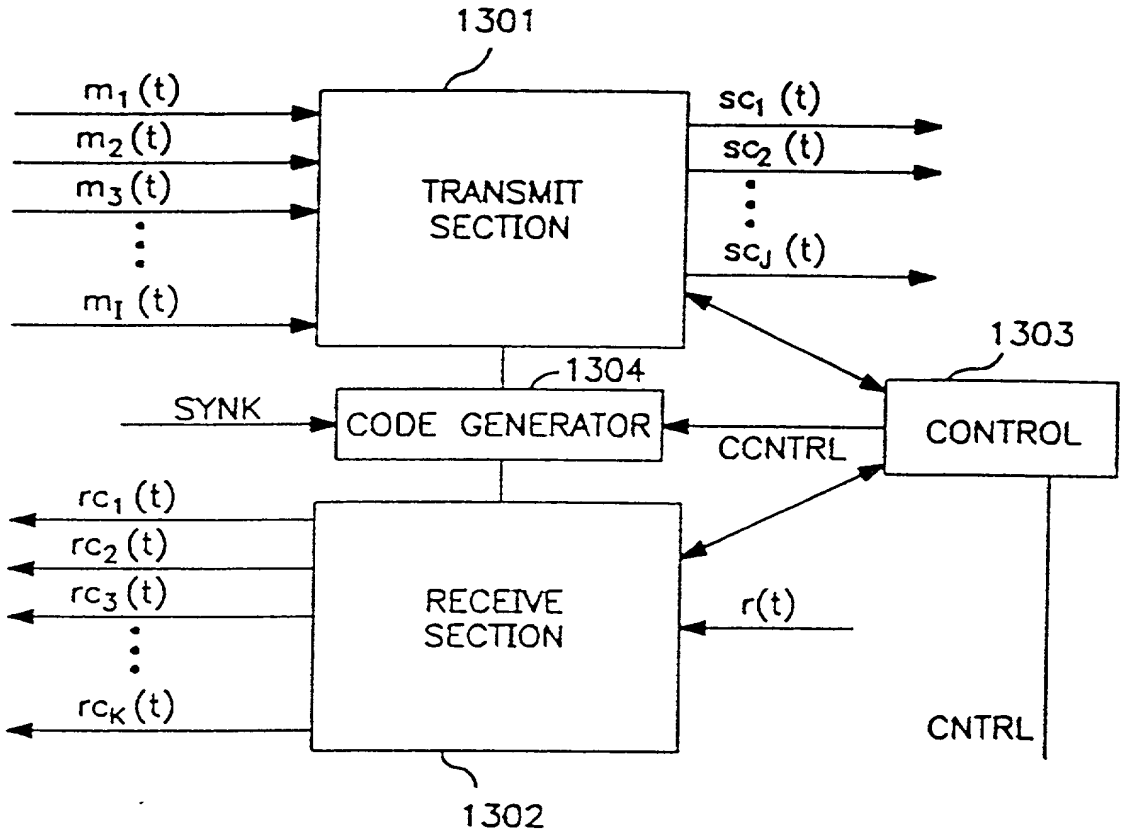

1301
$m_1(t)$
$m_2(t)$
$m_3(t)$
$m_I(t)$
TRANSMIT SECTION
$sc_1(t)$
$sc_2(t)$
$sc_J(t)$
1303
1304
SYNK
CODE GENERATOR
CCNTRL
CONTROL
$rc_1(t)$
$rc_2(t)$
$rc_3(t)$
$rc_K(t)$
RECEIVE SECTION
r(t)
CNTRL
1302

FIG. 13

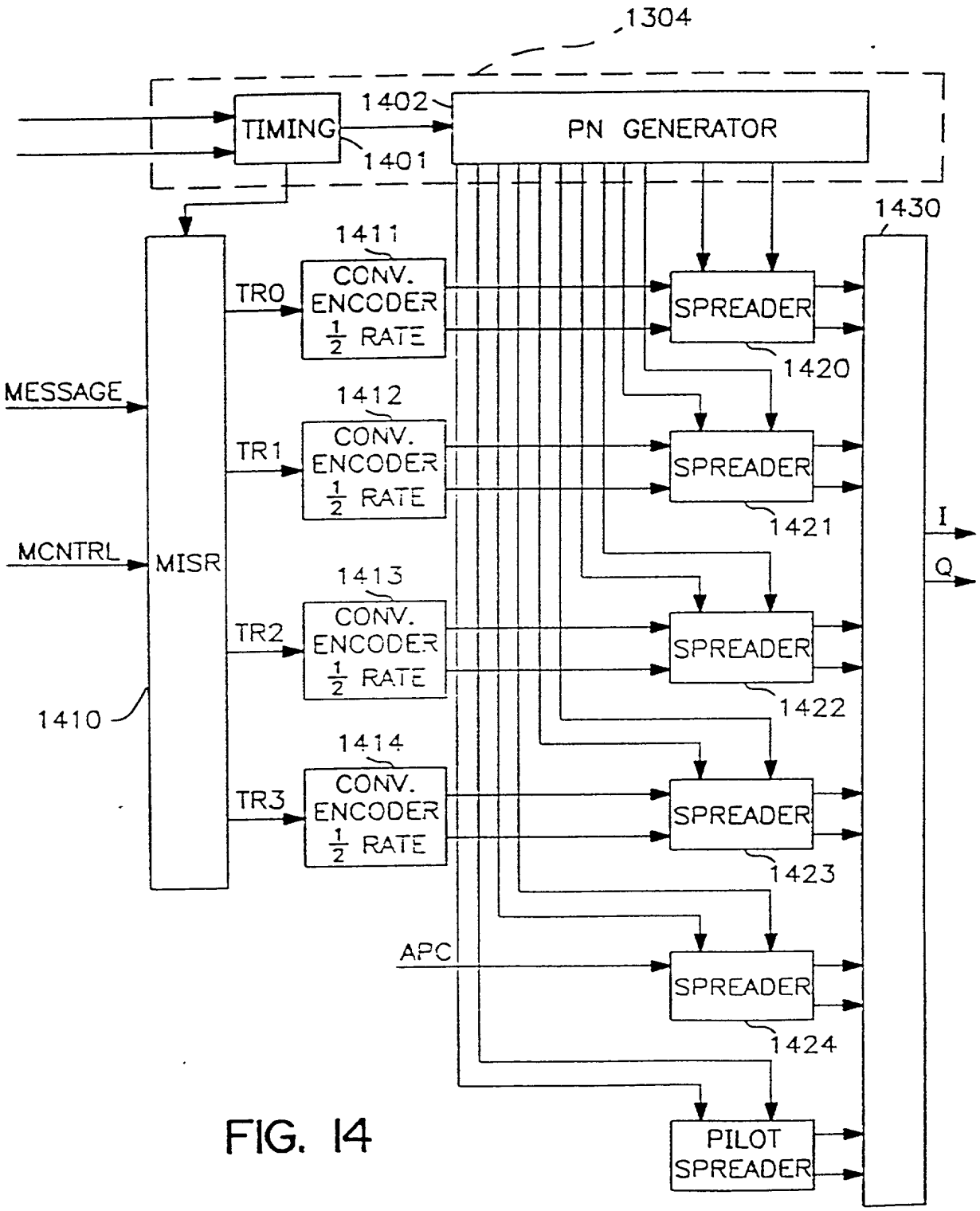

1304
TIMING
1402
1401
PN GENERATOR
1430
1411
CONV. ENCODER ½ RATE
TR0
SPREADER
1420
1412
CONV. ENCODER ½ RATE
TR1
SPREADER
1421
MESSAGE
MCNTRL
MISR
1413
CONV. ENCODER ½ RATE
TR2
SPREADER
1422
1410
1414
CONV. ENCODER ½ RATE
TR3
SPREADER
1423
APC
SPREADER
1424
PILOT SPREADER
I
Q

FIG. 14

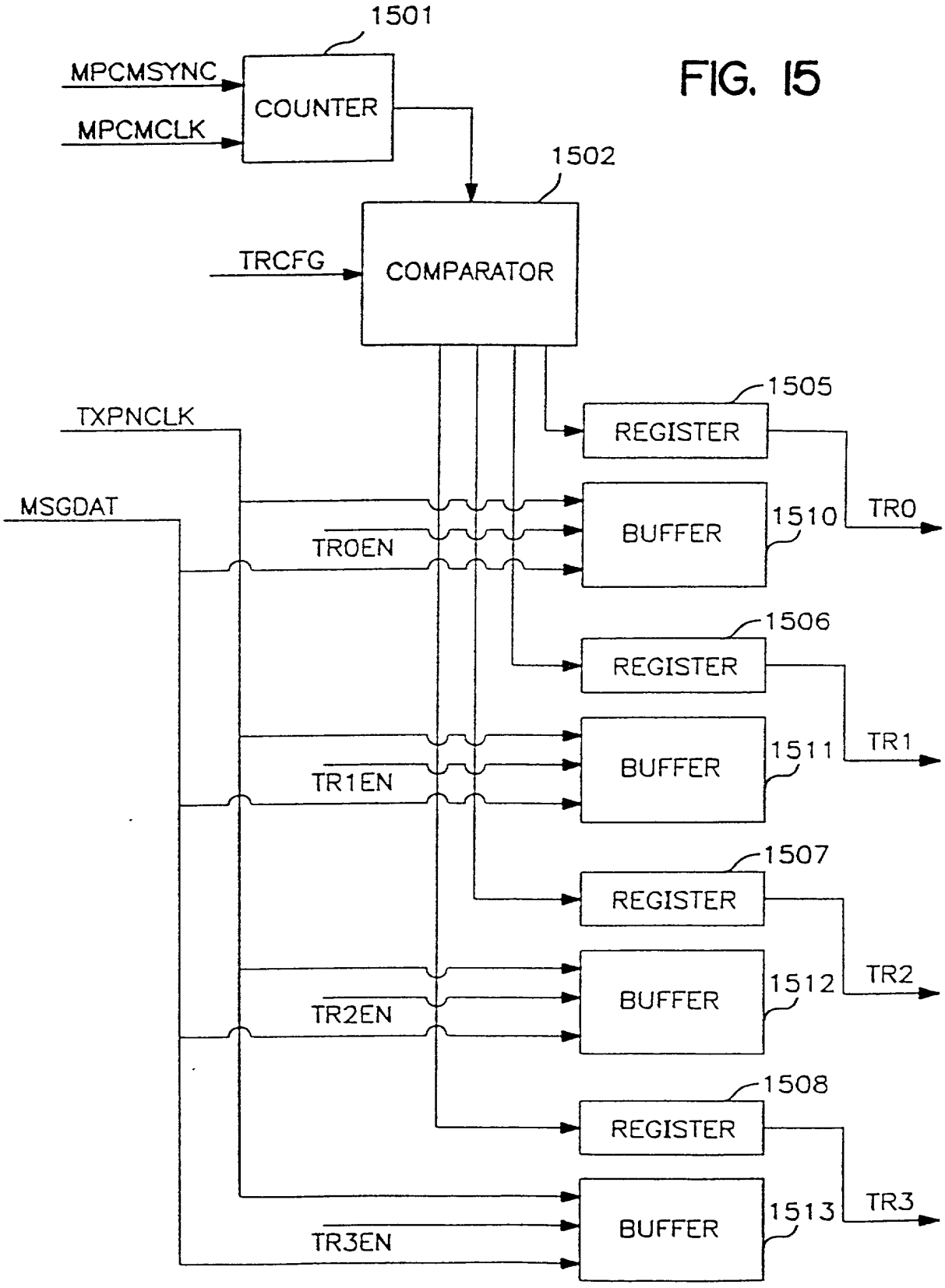

1501
MPCMSYNC
MPCMCLK
COUNTER
1502
TRCFG
COMPARATOR
1505
TXPNCLK
REGISTER
MSGDAT
BUFFER
1510
TR0
TR0EN
1506
REGISTER
BUFFER
1511
TR1
TR1EN
1507
REGISTER
BUFFER
1512
TR2
TR2EN
1508
REGISTER
BUFFER
1513
TR3
TR3EN

FIG. 15

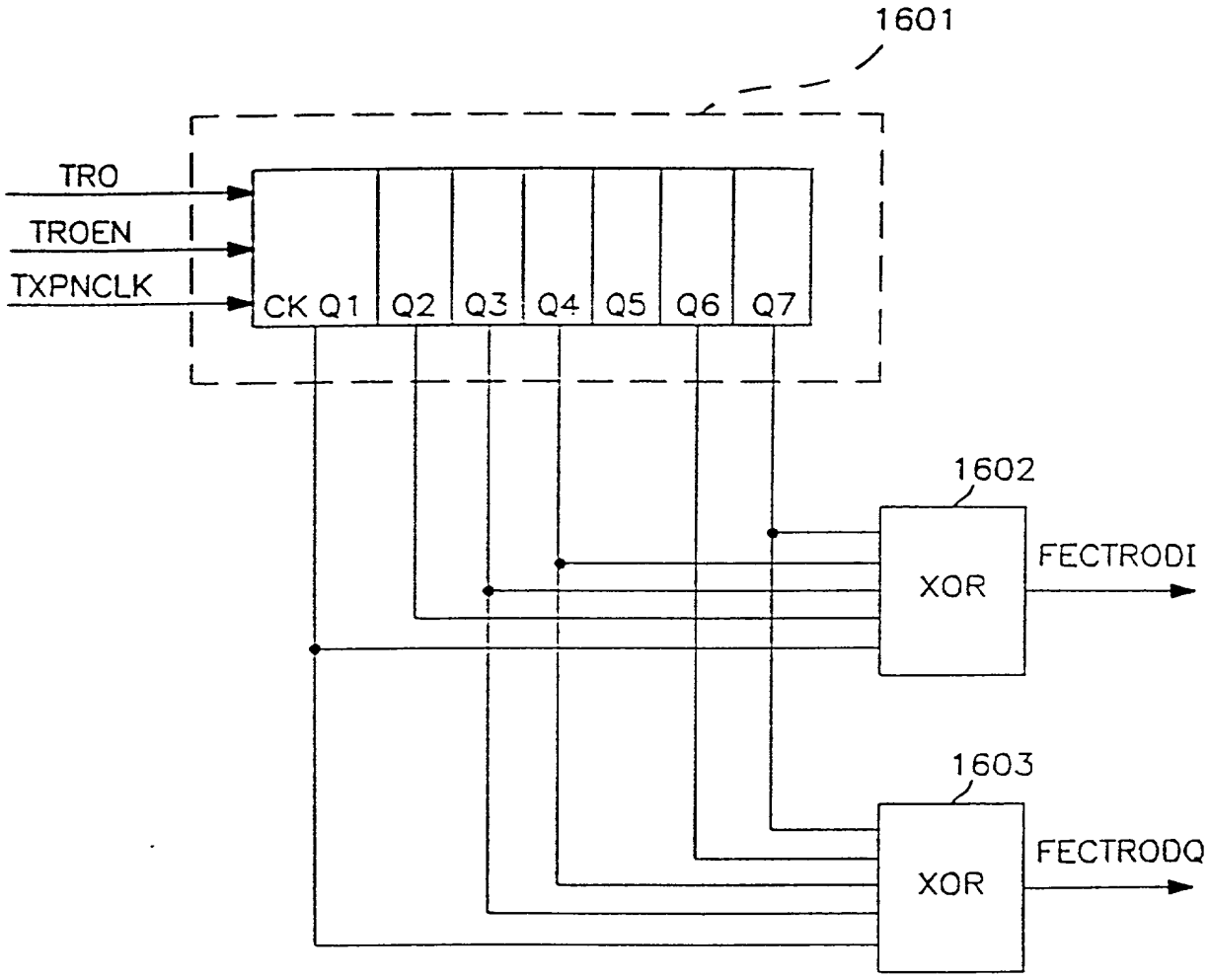

1601
TRO
TROEN
TXPNCLK
CK Q1
Q2
Q3
Q4
Q5
Q6
Q7
1602
XOR
FECTRODI
1603
XOR
FECTRODQ

FIG. 16

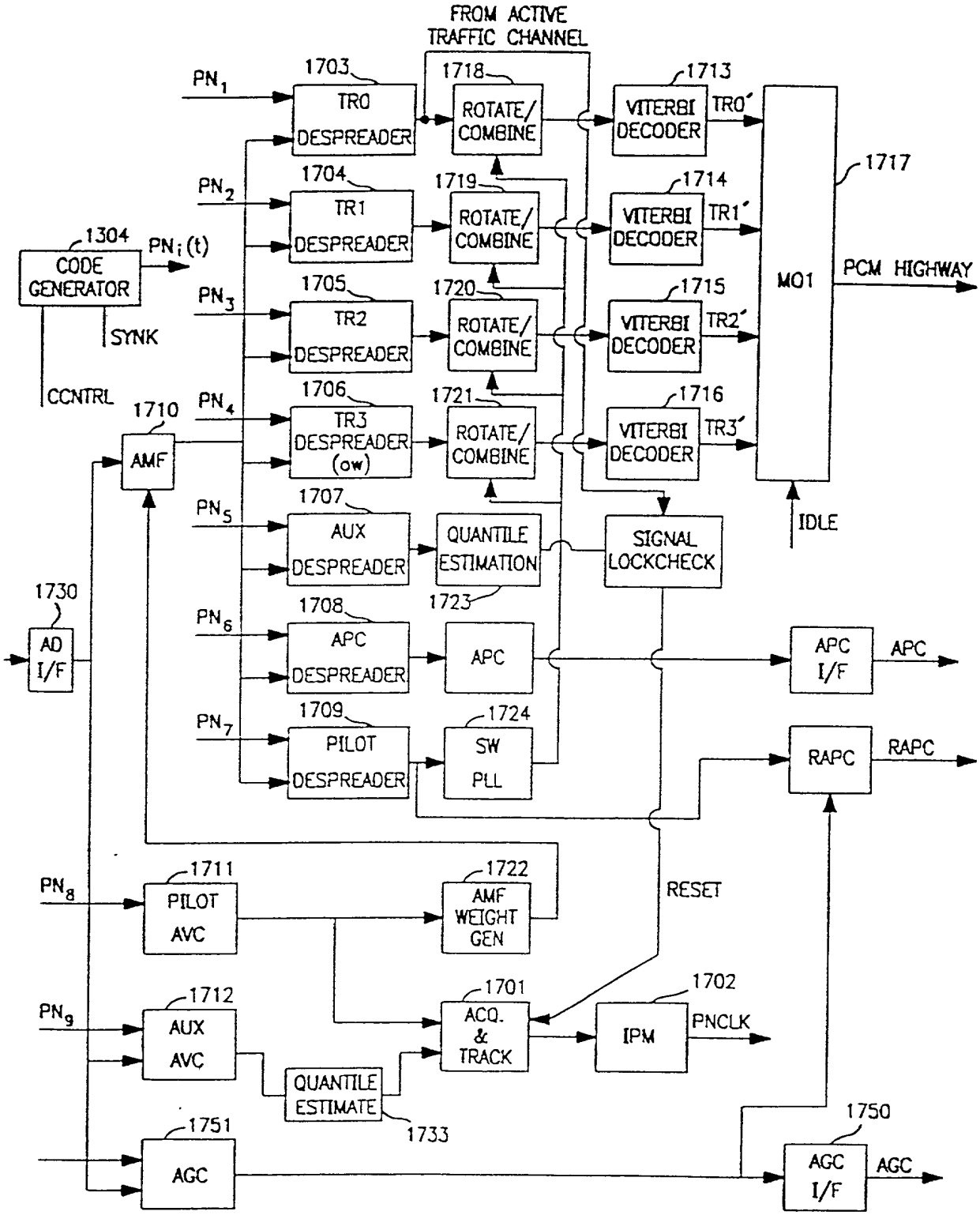

FROM ACTIVE TRAFFIC CHANNEL
PN1
1703
TR0 DESPREADER
1718
ROTATE/ COMBINE
1713
VITERBI DECODER
TR0'
PN2
1704
TR1 DESPREADER
1719
ROTATE/ COMBINE
1714
VITERBI DECODER
TR1'
1304
CODE GENERATOR
PNi(t)
SYNK
CCNTRL
PN3
1705
TR2 DESPREADER
1720
ROTATE/ COMBINE
1715
VITERBI DECODER
TR2'
PN4
1706
TR3 DESPREADER (ow)
1721
ROTATE/ COMBINE
1716
VITERBI DECODER
TR3'
1710
AMF
PN5
1707
AUX DESPREADER
QUANTILE ESTIMATION
1723
SIGNAL LOCKCHECK
1730
AD I/F
PN6
1708
APC DESPREADER
APC
APC I/F
APC
PN7
1709
PILOT DESPREADER
1724
SW PLL
RAPC
RAPC
1717
MO1
PCM HIGHWAY
IDLE
PN8
1711
PILOT AVC
1722
AMF WEIGHT GEN
RESET
PN9
1712
AUX AVC
1701
ACQ. & TRACK
1702
IPM
PNCLK
QUANTILE ESTIMATE
1733
1751
AGC
1750
AGC I/F
AGC

FIG. 17

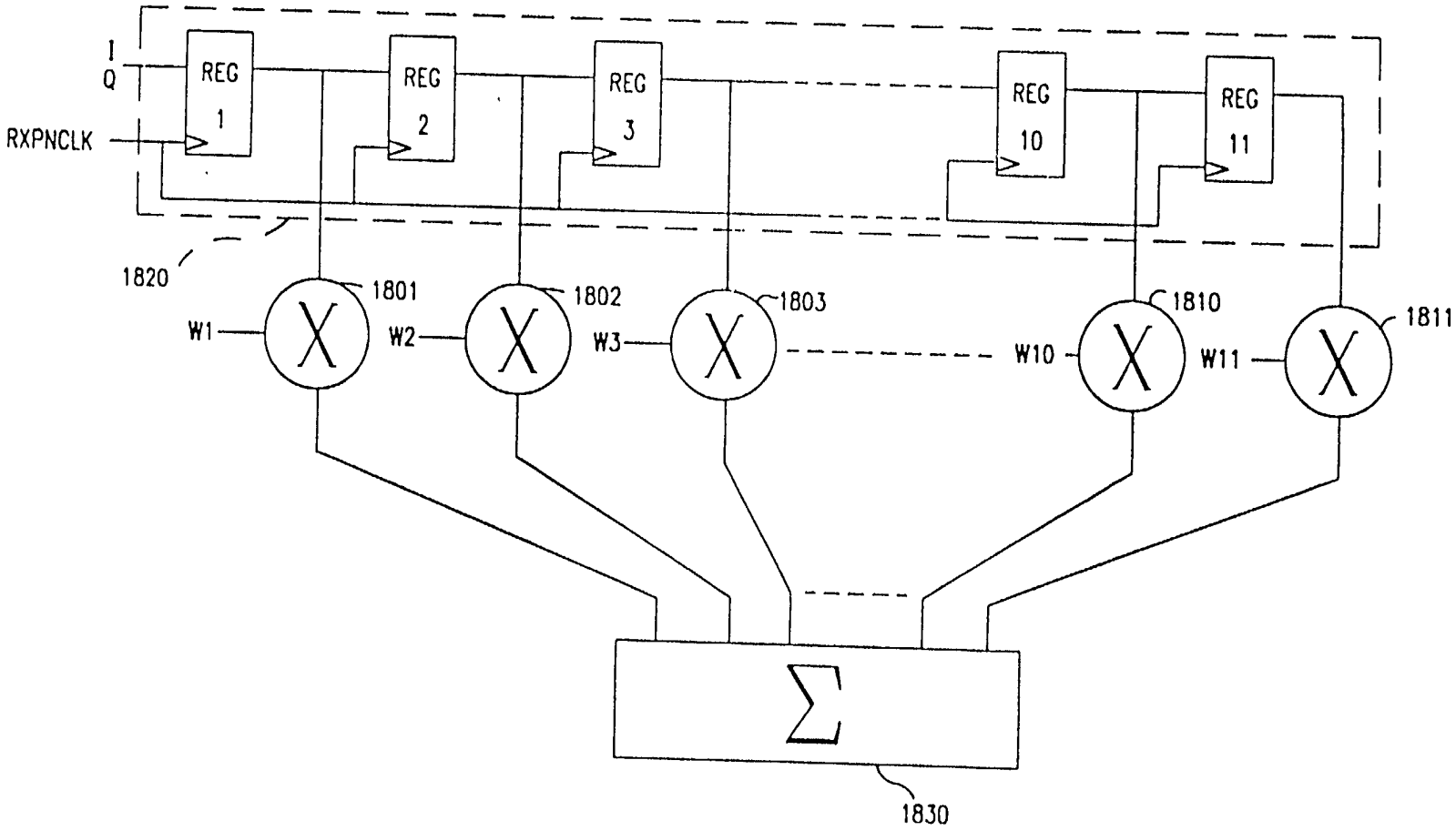

I
Q
RXPNCLK
REG 1
REG 2
REG 3
REG 10
REG 11
1820
1801
1802
1803
1810
1811
W1
W2
W3
W10
W11
Σ
1830

FIG. 18

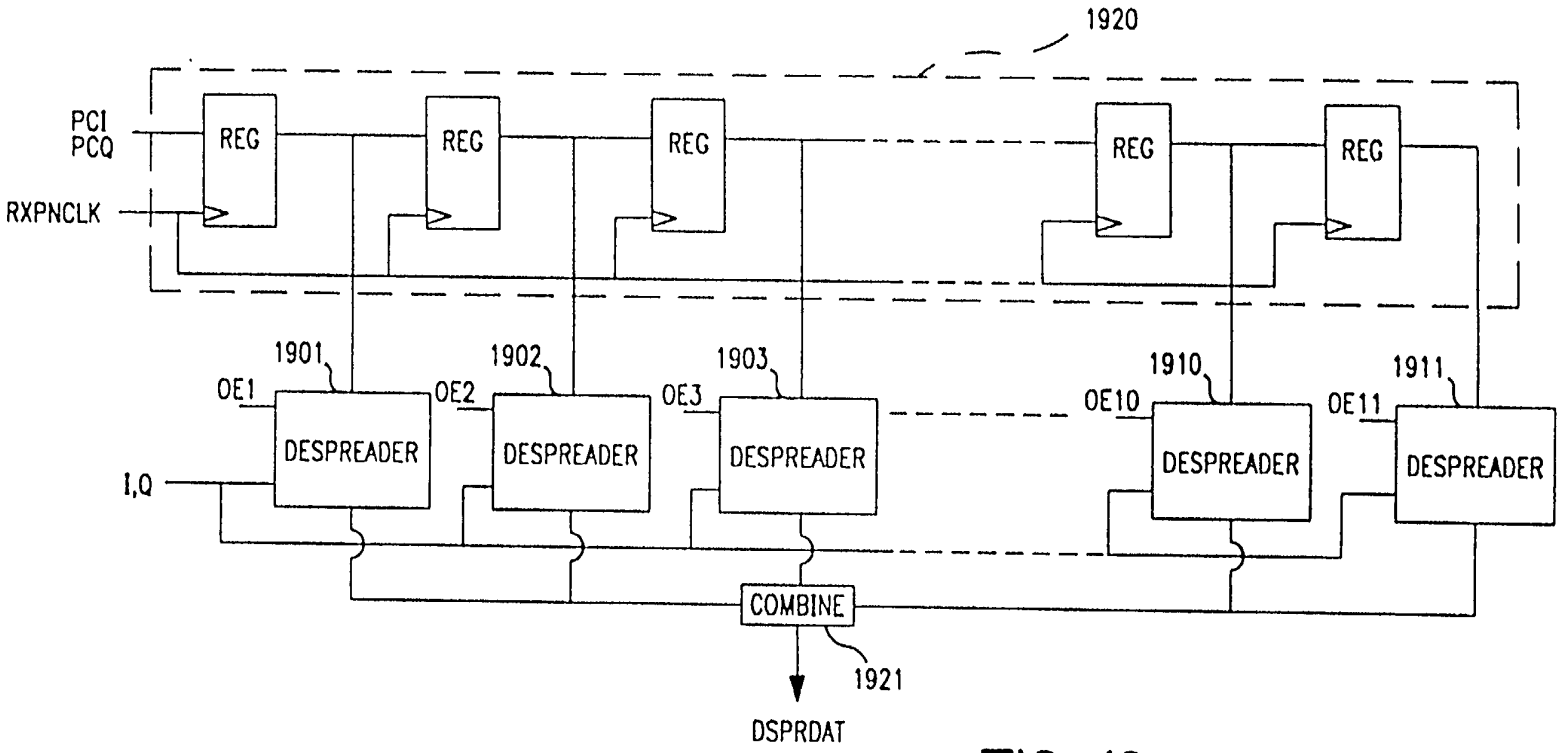

1920
PCI
PCQ
RXPNCLK
REG
REG
REG
REG
REG
1901
1902
1903
1910
1911
OE1
OE2
OE3
OE10
OE11
DESPREADER
DESPREADER
DESPREADER
DESPREADER
DESPREADER
I,Q
COMBINE
1921
DSPRDAT

FIG. 19

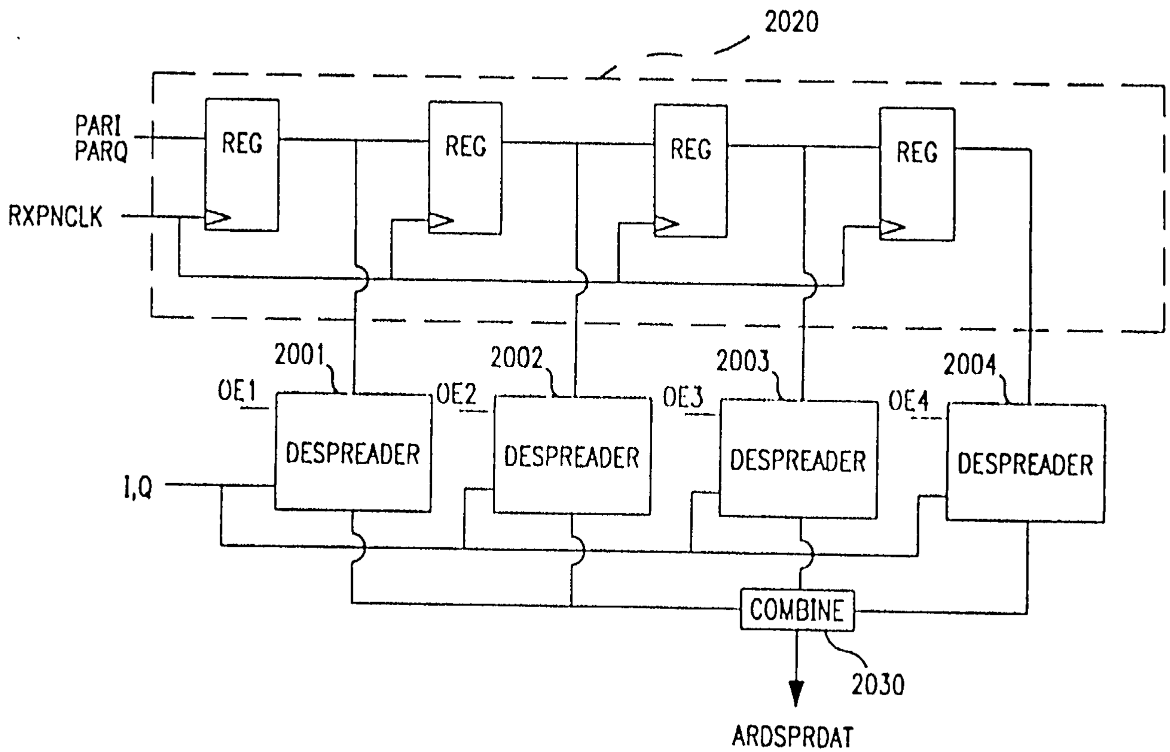

2020
PARI
PARQ
RXPNCLK
REG
REG
REG
REG
2001
2002
2003
2004
OE1
OE2
OE3
OE4
I,Q
DESPREADER
DESPREADER
DESPREADER
DESPREADER
COMBINE
2030
ARDSPRDAT

FIG. 20

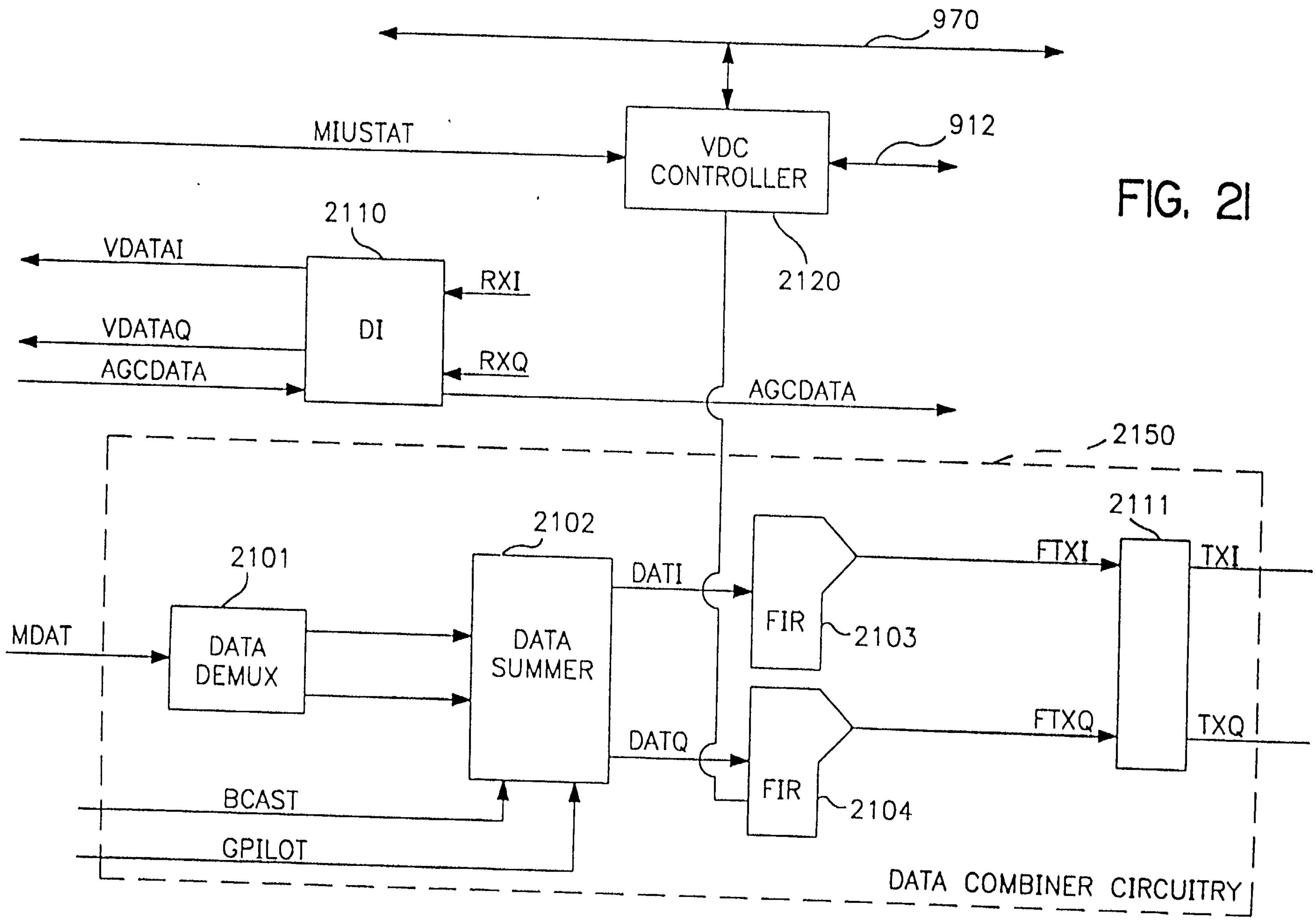


FIG. 2I

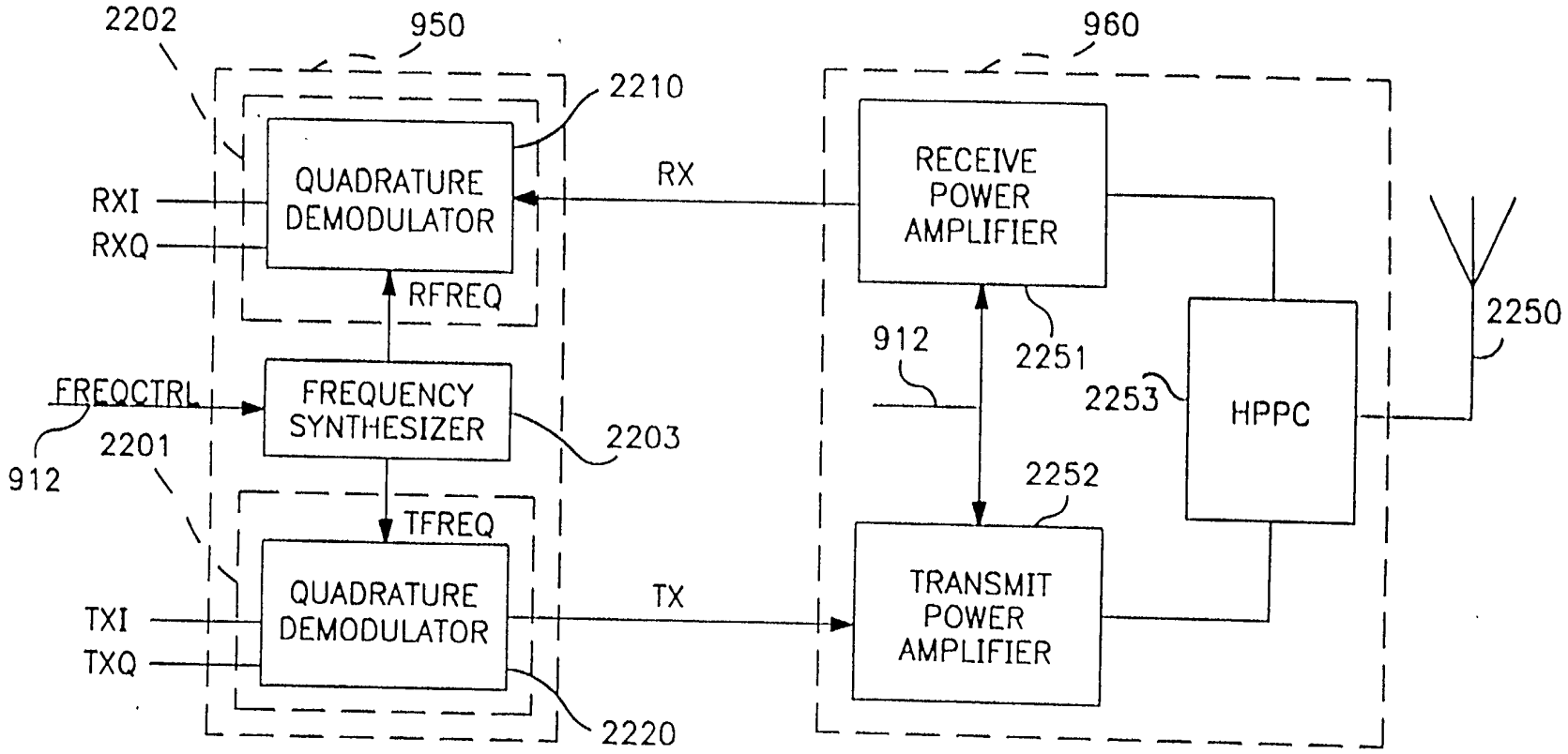


FIG. 22

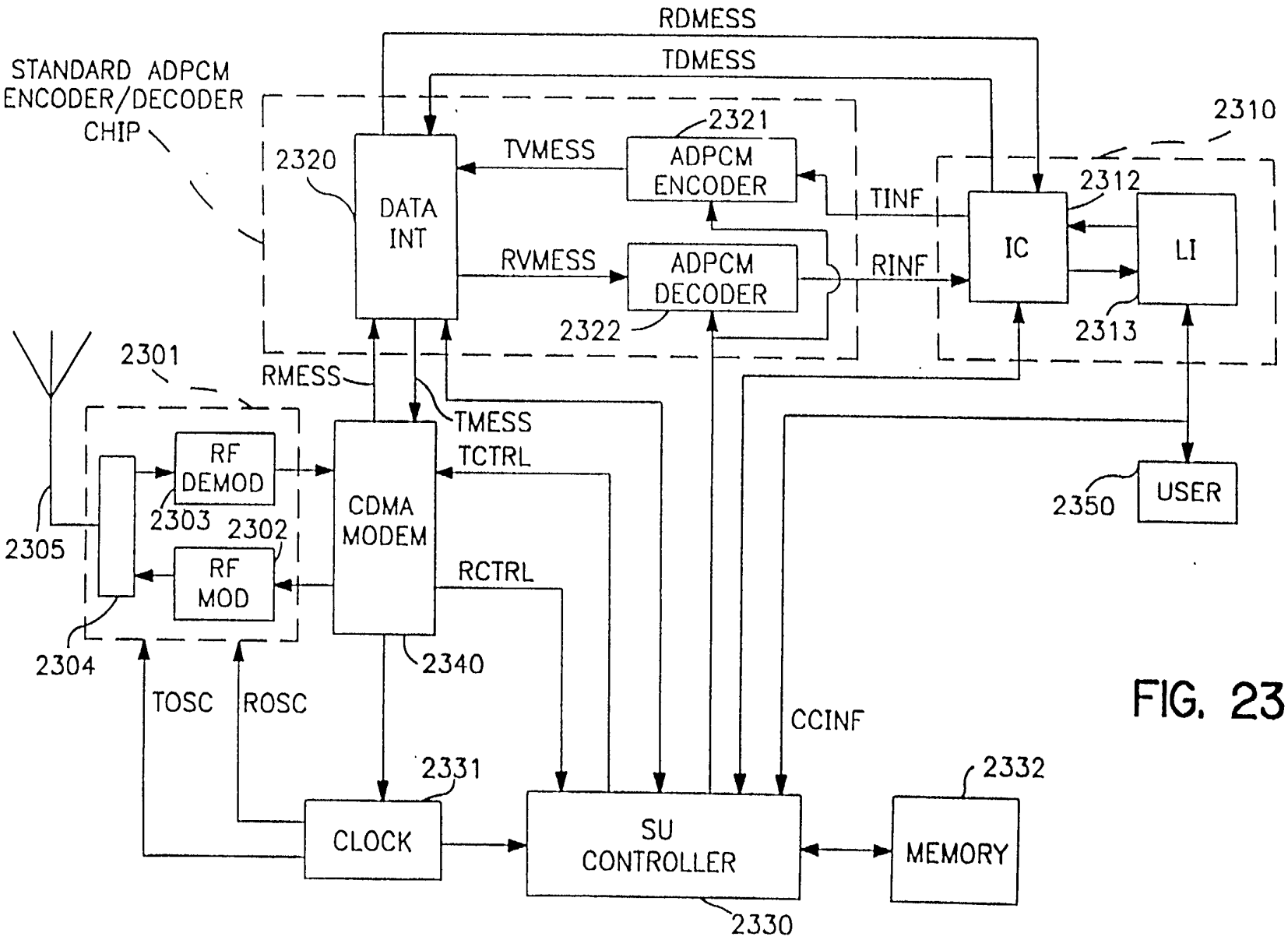

RDMESS
TDMESS
STANDARD ADPCM ENCODER/DECODER CHIP
2310
2321
2320
TVMESS
ADPCM ENCODER
DATA INT
TINF
2312
IC
LI
RVMESS
ADPCM DECODER
RINF
2322
2313
2301
RMESS
TMESS
TCTRL
RF DEMOD
CDMA MODEM
2303
2302
2350
USER
2305
RF MOD
RCTRL
2304
2340
TOSC
ROSC
CCINF
2331
2332
CLOCK
SU CONTROLLER
MEMORY
2330

FIG. 23

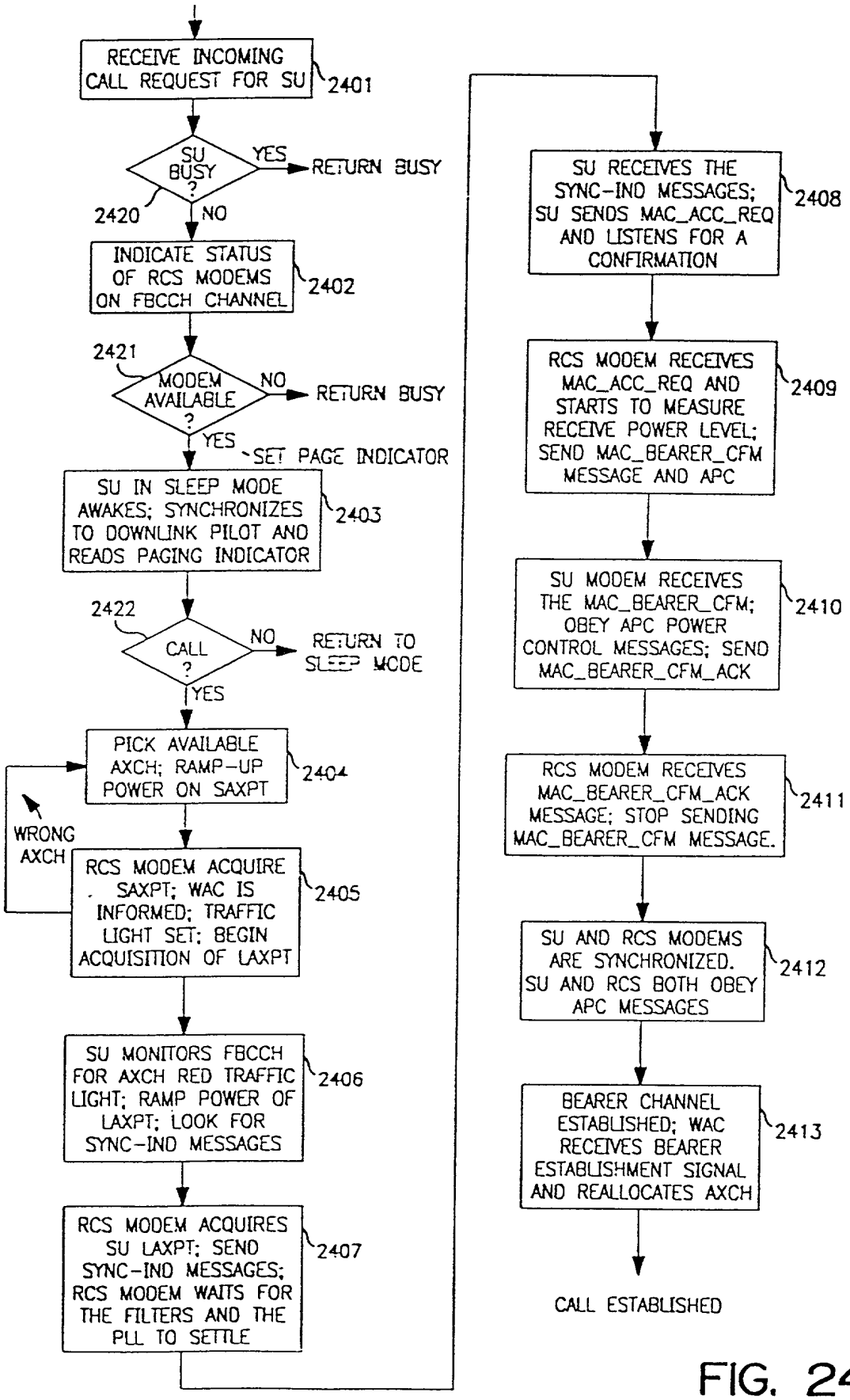

RECEIVE INCOMING CALL REQUEST FOR SU
2401
SU BUSY ?
YES
RETURN BUSY
2420
NO
INDICATE STATUS OF RCS MODEMS ON FBCCH CHANNEL
2402
2421
MODEM AVAILABLE ?
NO
RETURN BUSY
YES
SET PAGE INDICATOR
SU IN SLEEP MODE AWAKES; SYNCHRONIZES TO DOWNLINK PILOT AND READS PAGING INDICATOR
2403
2422
CALL ?
NO
RETURN TO SLEEP MODE
YES
PICK AVAILABLE AXCH; RAMP-UP POWER ON SAXPT
2404
WRONG AXCH
RCS MODEM ACQUIRE SAXPT; WAC IS INFORMED; TRAFFIC LIGHT SET; BEGIN ACQUISITION OF LAXPT
2405
SU MONITORS FBCCH FOR AXCH RED TRAFFIC LIGHT; RAMP POWER OF LAXPT; LOOK FOR SYNC-IND MESSAGES
2406
RCS MODEM ACQUIRES SU LAXPT; SEND SYNC-IND MESSAGES; RCS MODEM WAITS FOR THE FILTERS AND THE PLL TO SETTLE
2407
SU RECEIVES THE SYNC-IND MESSAGES; SU SENDS MAC_ACC_REQ AND LISTENS FOR A CONFIRMATION
2408
RCS MODEM RECEIVES MAC_ACC_REQ AND STARTS TO MEASURE RECEIVE POWER LEVEL; SEND MAC_BEARER_CFM MESSAGE AND APC
2409
SU MODEM RECEIVES THE MAC_BEARER_CFM; OBEY APC POWER CONTROL MESSAGES; SEND MAC_BEARER_CFM_ACK
2410
RCS MODEM RECEIVES MAC_BEARER_CFM_ACK MESSAGE; STOP SENDING MAC_BEARER_CFM MESSAGE.
2411
SU AND RCS MODEMS ARE SYNCHRONIZED. SU AND RCS BOTH OBEY APC MESSAGES
2412
BEARER CHANNEL ESTABLISHED; WAC RECEIVES BEARER ESTABLISHMENT SIGNAL AND REALLOCATES AXCH
2413
CALL ESTABLISHED

FIG. 24

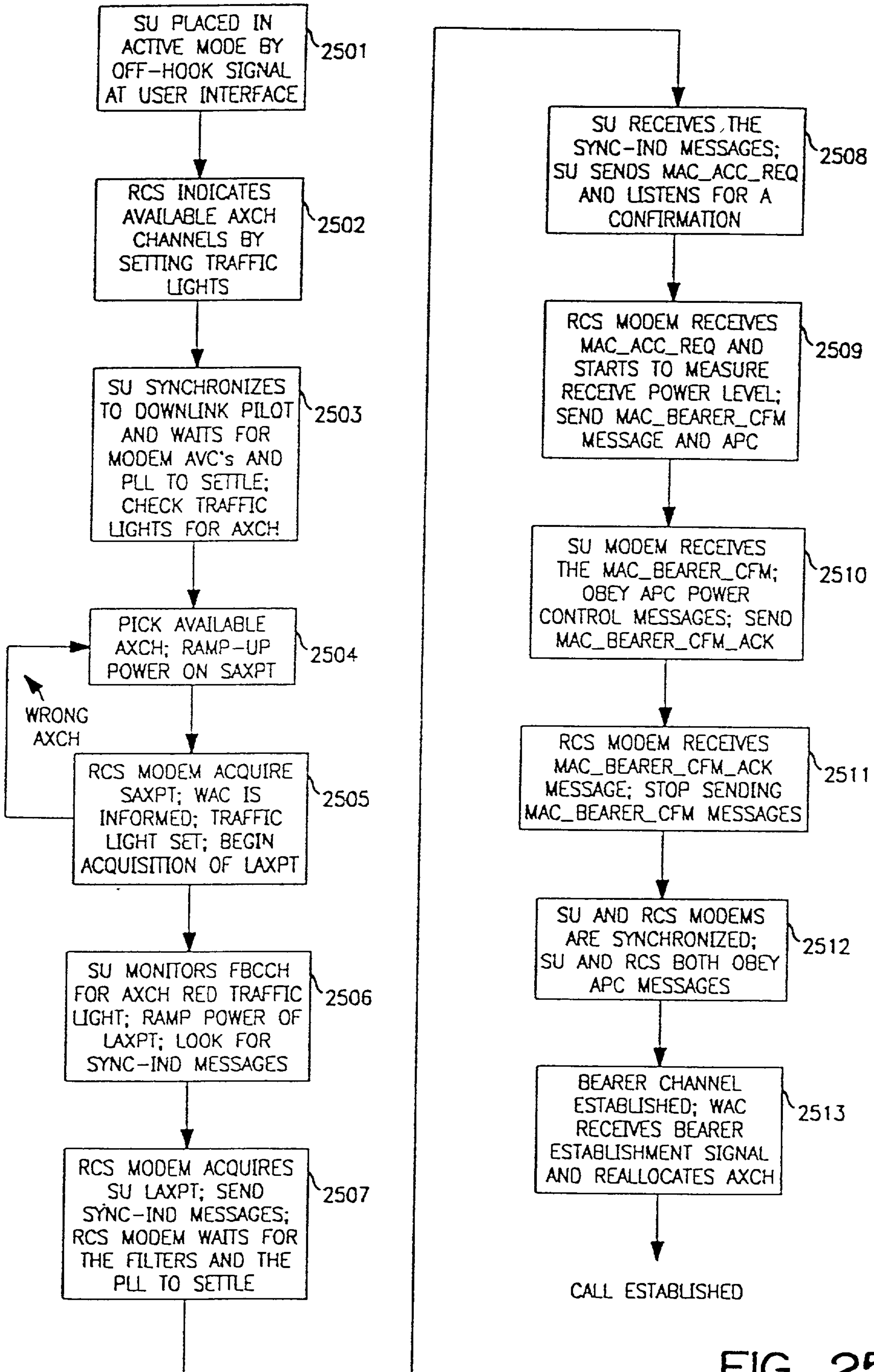

SU PLACED IN ACTIVE MODE BY OFF-HOOK SIGNAL AT USER INTERFACE
2501
RCS INDICATES AVAILABLE AXCH CHANNELS BY SETTING TRAFFIC LIGHTS
2502
SU SYNCHRONIZES TO DOWNLINK PILOT AND WAITS FOR MODEM AVC's AND PLL TO SETTLE; CHECK TRAFFIC LIGHTS FOR AXCH
2503
PICK AVAILABLE AXCH; RAMP-UP POWER ON SAXPT
2504
WRONG AXCH
RCS MODEM ACQUIRE SAXPT; WAC IS INFORMED; TRAFFIC LIGHT SET; BEGIN ACQUISITION OF LAXPT
2505
SU MONITORS FBCCH FOR AXCH RED TRAFFIC LIGHT; RAMP POWER OF LAXPT; LOOK FOR SYNC-IND MESSAGES
2506
RCS MODEM ACQUIRES SU LAXPT; SEND SYNC-IND MESSAGES; RCS MODEM WAITS FOR THE FILTERS AND THE PLL TO SETTLE
2507
SU RECEIVES THE SYNC-IND MESSAGES; SU SENDS MAC_ACC_REQ AND LISTENS FOR A CONFIRMATION
2508
RCS MODEM RECEIVES MAC_ACC_REQ AND STARTS TO MEASURE RECEIVE POWER LEVEL; SEND MAC_BEARER_CFM MESSAGE AND APC
2509
SU MODEM RECEIVES THE MAC_BEARER_CFM; OBEY APC POWER CONTROL MESSAGES; SEND MAC_BEARER_CFM_ACK
2510
RCS MODEM RECEIVES MAC_BEARER_CFM_ACK MESSAGE; STOP SENDING MAC_BEARER_CFM MESSAGES
2511
SU AND RCS MODEMS ARE SYNCHRONIZED; SU AND RCS BOTH OBEY APC MESSAGES
2512
BEARER CHANNEL ESTABLISHED; WAC RECEIVES BEARER ESTABLISHMENT SIGNAL AND REALLOCATES AXCH
2513
CALL ESTABLISHED

FIG. 25

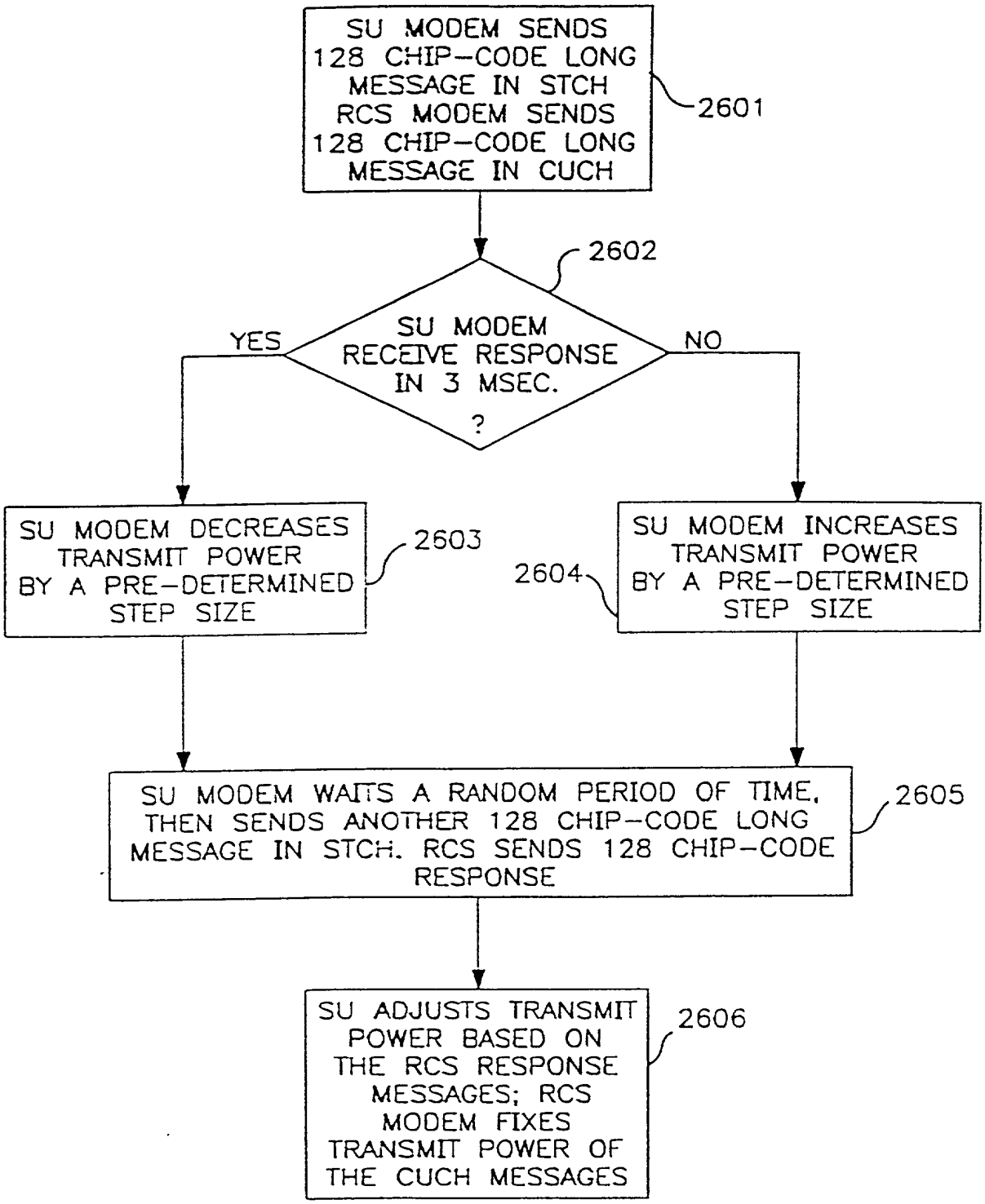

SU MODEM SENDS 128 CHIP-CODE LONG MESSAGE IN STCH RCS MODEM SENDS 128 CHIP-CODE LONG MESSAGE IN CUCH
2601
2602
SU MODEM RECEIVE RESPONSE IN 3 MSEC. ?
YES
NO
SU MODEM DECREASES TRANSMIT POWER BY A PRE-DETERMINED STEP SIZE
2603
SU MODEM INCREASES TRANSMIT POWER BY A PRE-DETERMINED STEP SIZE
2604
SU MODEM WAITS A RANDOM PERIOD OF TIME, THEN SENDS ANOTHER 128 CHIP-CODE LONG MESSAGE IN STCH. RCS SENDS 128 CHIP-CODE RESPONSE
2605
SU ADJUSTS TRANSMIT POWER BASED ON THE RCS RESPONSE MESSAGES; RCS MODEM FIXES TRANSMIT POWER OF THE CUCH MESSAGES
2606

FIG. 26

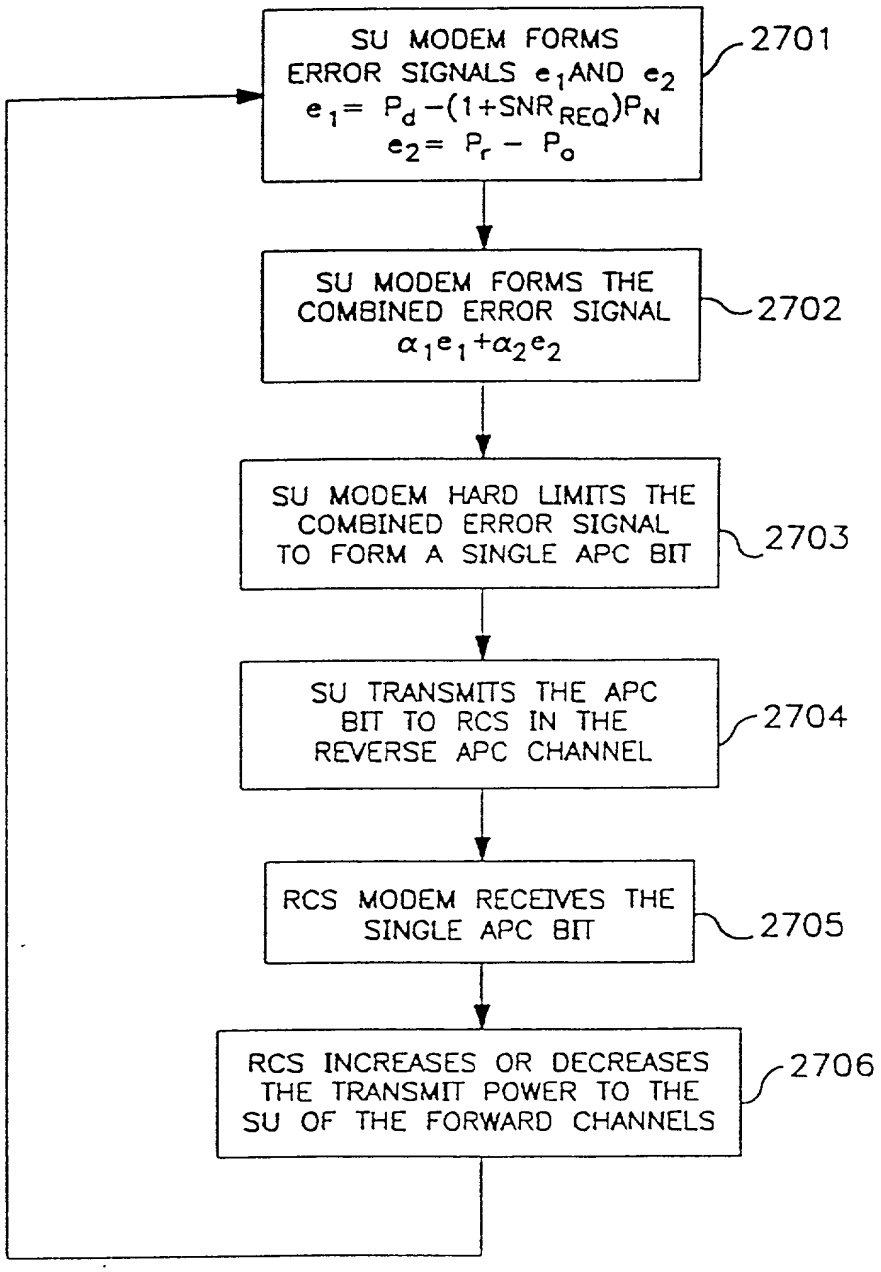

SU MODEM FORMS ERROR SIGNALS e_1 AND e_2
$e_1 = P_d - (1+SNR_{REQ})P_N$
$e_2 = P_r - P_o$
2701
SU MODEM FORMS THE COMBINED ERROR SIGNAL
$\alpha_1 e_1 + \alpha_2 e_2$
2702
SU MODEM HARD LIMITS THE COMBINED ERROR SIGNAL TO FORM A SINGLE APC BIT
2703
SU TRANSMITS THE APC BIT TO RCS IN THE REVERSE APC CHANNEL
2704
RCS MODEM RECEIVES THE SINGLE APC BIT
2705
RCS INCREASES OR DECREASES THE TRANSMIT POWER TO THE SU OF THE FORWARD CHANNELS
2706

FIG. 27

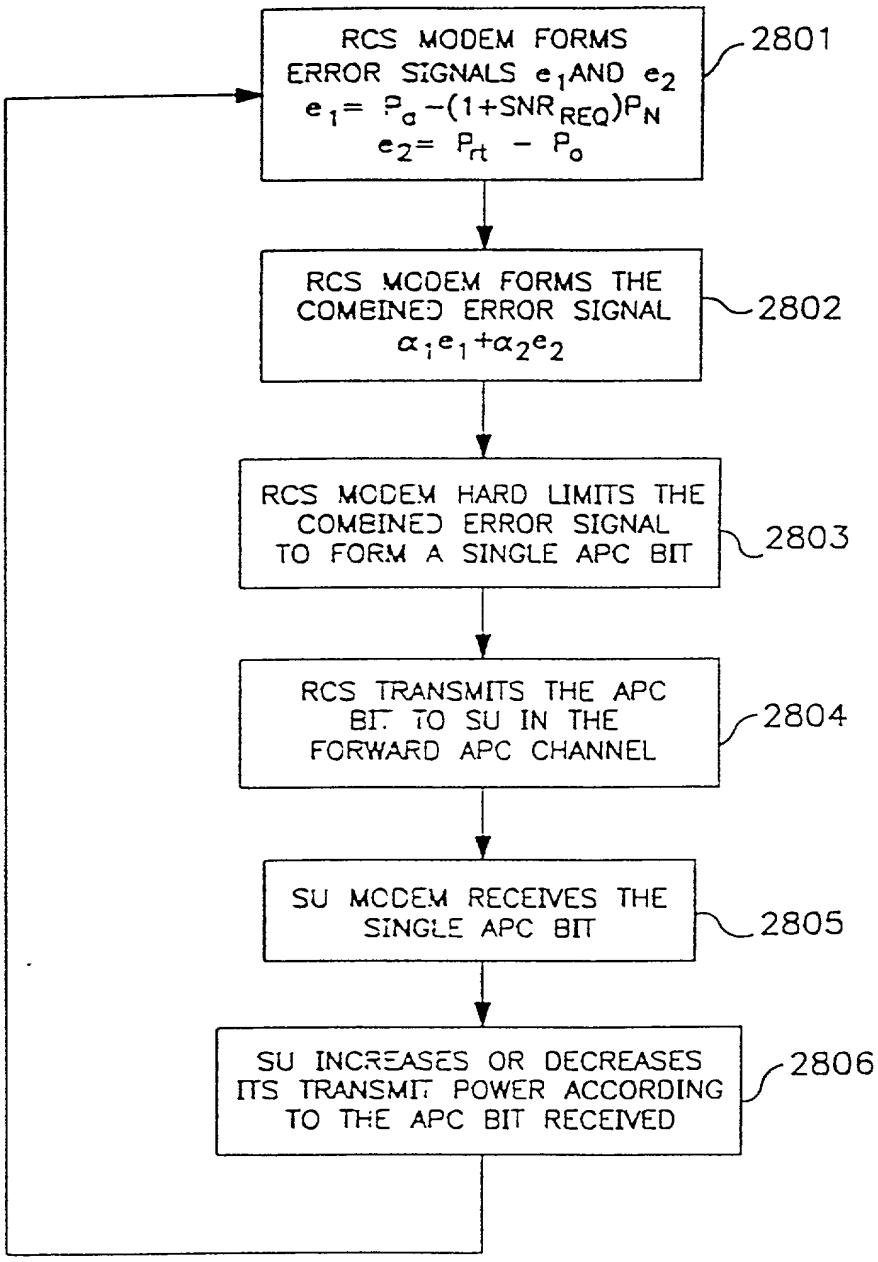

RCS MODEM FORMS ERROR SIGNALS e_1 AND e_2
$e_1 = P_a - (1+SNR_{REQ})P_N$
$e_2 = P_{rt} - P_o$
2801
RCS MODEM FORMS THE COMBINED ERROR SIGNAL
$\alpha_1 e_1 + \alpha_2 e_2$
2802
RCS MODEM HARD LIMITS THE COMBINED ERROR SIGNAL TO FORM A SINGLE APC BIT
2803
RCS TRANSMITS THE APC BIT TO SU IN THE FORWARD APC CHANNEL
2804
SU MODEM RECEIVES THE SINGLE APC BIT
2805
SU INCREASES OR DECREASES ITS TRANSMIT POWER ACCORDING TO THE APC BIT RECEIVED
2806

FIG. 28

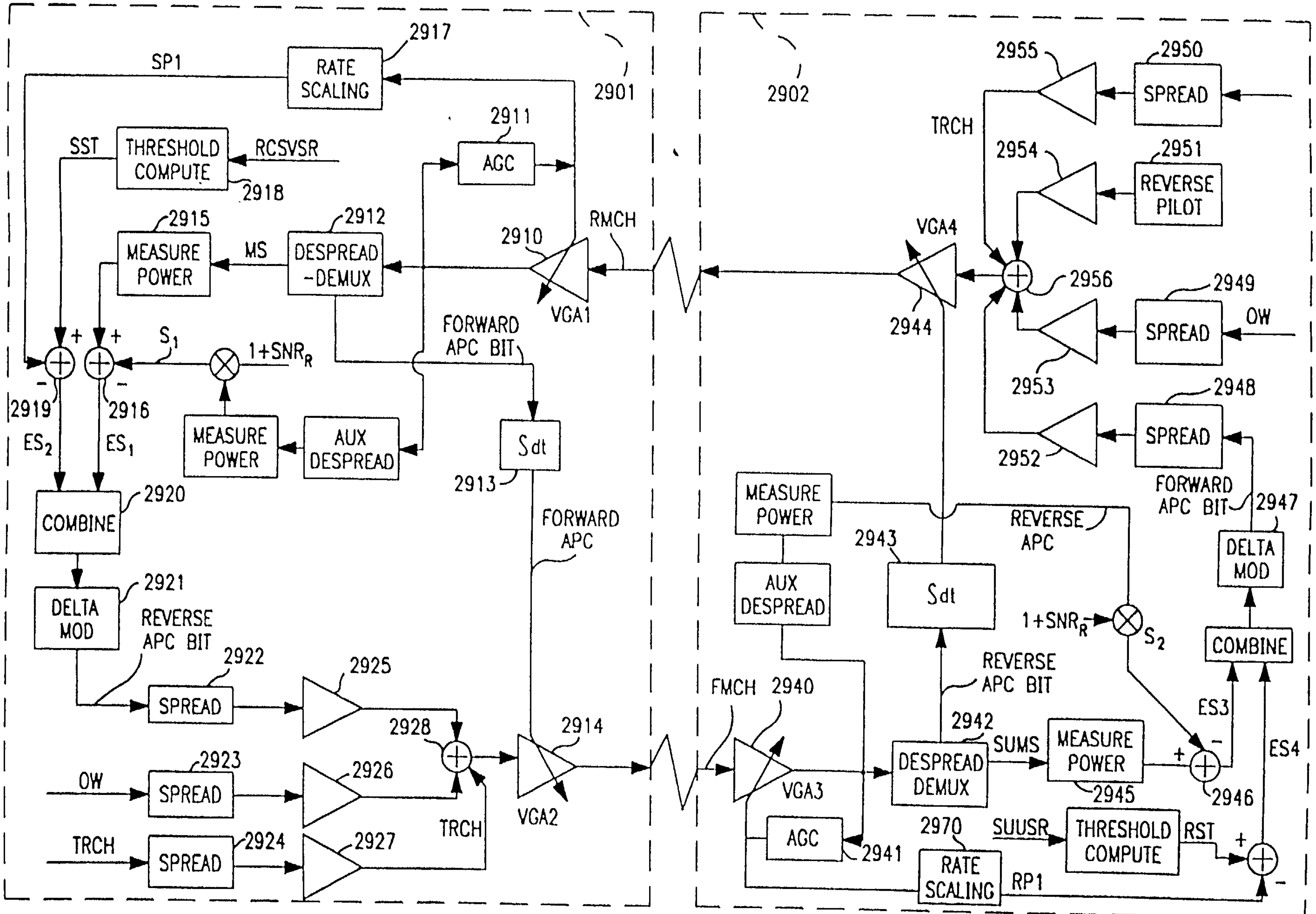

2901
2902
SP1
RATE SCALING
2917
SST
THRESHOLD COMPUTE
RCSVSR
2918
AGC
2911
MEASURE POWER
2915
MS
DESPREAD -DEMUX
2912
2910
RMCH
VGA1
S1
1+SNR_R
2919
2916
ES2
ES1
MEASURE POWER
AUX DESPREAD
FORWARD APC BIT
Sdt
2913
COMBINE
2920
FORWARD APC
DELTA MOD
2921
REVERSE APC BIT
2922
SPREAD
2925
2928
2914
VGA2
OW
SPREAD
2923
2926
TRCH
SPREAD
2924
2927
TRCH
2955
SPREAD
2950
TRCH
2954
REVERSE PILOT
2951
VGA4
2956
SPREAD
2949
OW
2944
2953
SPREAD
2948
2952
MEASURE POWER
FORWARD APC BIT
2947
REVERSE APC
2943
DELTA MOD
AUX DESPREAD
Sdt
1+SNR_R
S2
COMBINE
REVERSE APC BIT
ES3
FMCH
2940
2942
SUMS
MEASURE POWER
ES4
DESPREAD DEMUX
VGA3
2945
2946
AGC
2941
2970
SUUSR
THRESHOLD COMPUTE
RST
RATE SCALING
RP1

FIG. 29

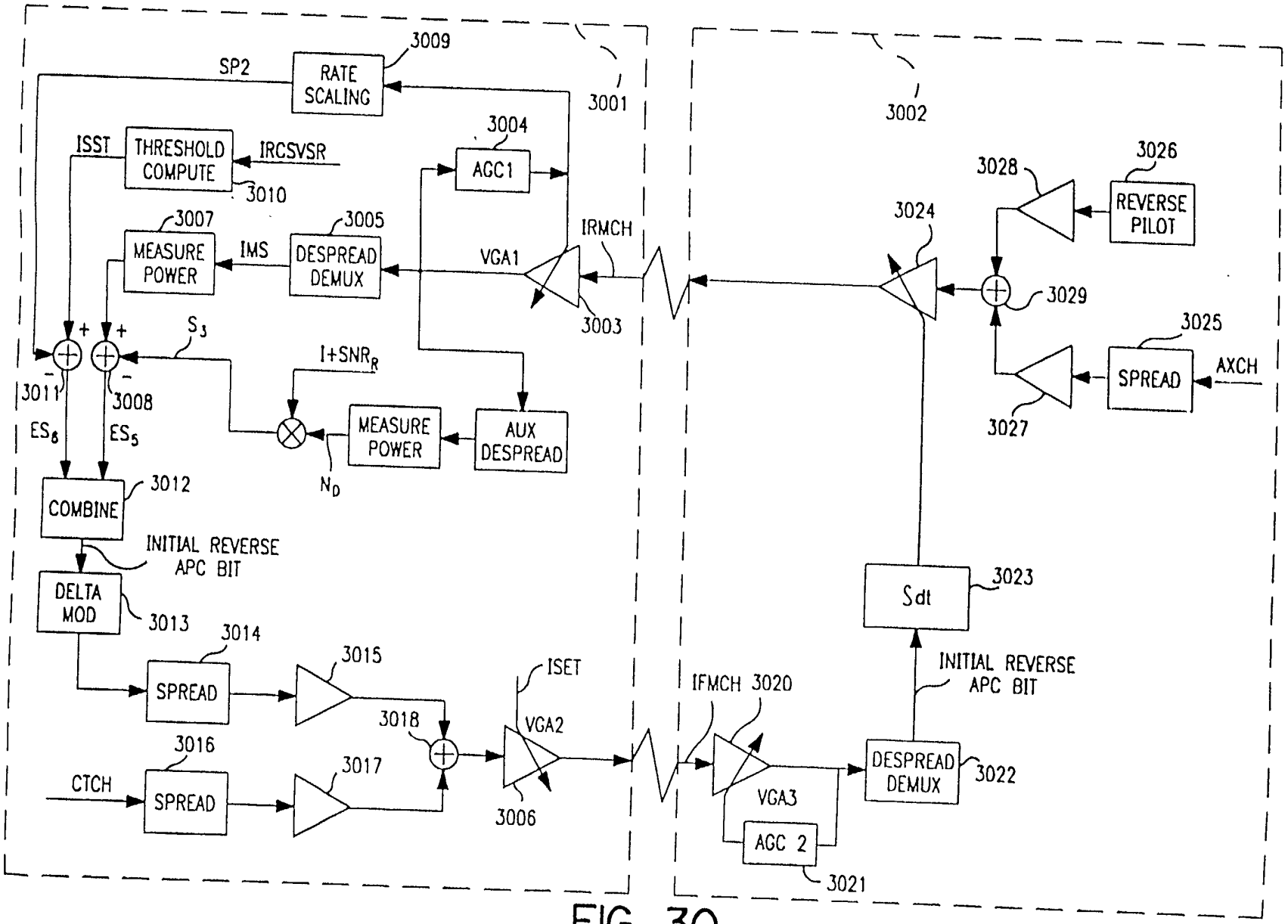

3009
SP2
RATE SCALING
3001
3002
3004
ISST
THRESHOLD COMPUTE
IRCSVSR
3010
AGC1
3026
3028
REVERSE PILOT
3024
3007
MEASURE POWER
IMS
3005
DESPREAD DEMUX
VGA1
IRMCH
3003
3029
3025
S_3
I+SNR$_R$
SPREAD
AXCH
3027
3011
3008
ES_6
ES_5
MEASURE POWER
AUX DESPREAD
N_D
3012
COMBINE
INITIAL REVERSE APC BIT
3023
Sdt
DELTA MOD
3013
3014
3015
ISET
IFMCH 3020
INITIAL REVERSE APC BIT
SPREAD
3018
VGA2
3016
3017
CTCH
SPREAD
VGA3
DESPREAD DEMUX
3022
AGC 2
3006
3021

FIG. 30